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INSTRUCTION MANUAL

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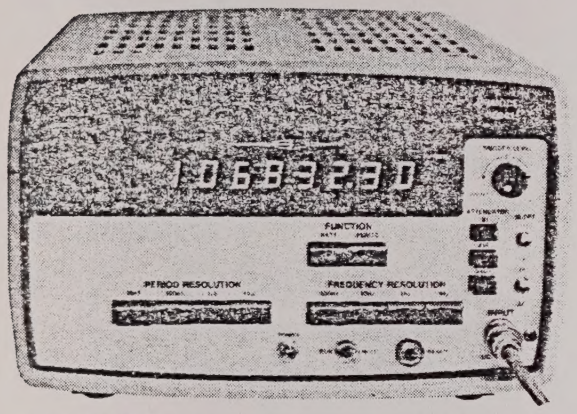
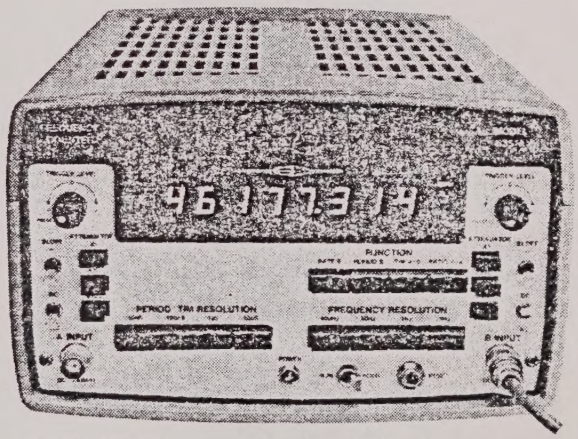
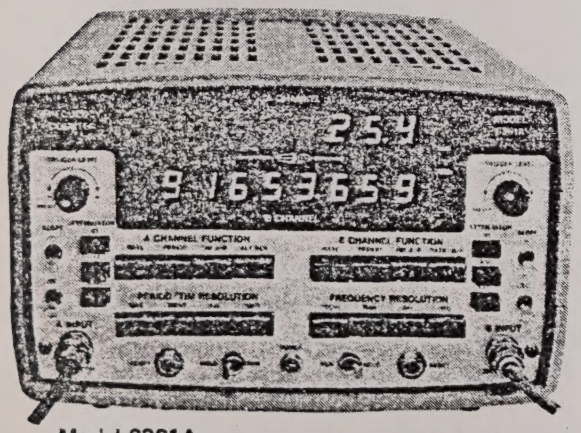


Model 6341A



Model 6351A



Model 6361A

MODEL 6341A
MODEL 6351A
MODEL 6361A

FREQUENCY COUNTERS

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SYSTRON DONNER

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CHAPTER 1

GENERAL INFORMATION

1.1 INTRODUCTION

The 63X1A Series Counter Timers provide a unique measurement concept for bench top Universal Counter/Timers. Three models comprise the 63X1A series starting with the 6341A, a 100 MHz /10 ns Counter Timer. The 6351A 100 MHz/10 ns Universal Counter Timer and the 6361A 100 MHz /10 ns Dual Universal Counter Timer complete the series. All provide input signal conditioning for trigger level control, preset control, attenuation, slop selection and ac/dc coupling.

The Model 6341A is the basic unit configured for Rate (frequency) and Period measurements. A 100 MHz/10 ns single channel counter with 10 mV sensitivity, full input conditioning, and selectable resolution of 0.1 Hz to 100 Hz in decade steps (frequency mode) or 10 ns to 10 μs in decade steps (period mode). Large 8 digit LED display with leading zero suppression, automatically positioned decimal point and off scale, gate, and measurement units kHz, ms, μs annunciators provide unambiguous visual display of the measurement. Other features include front panel mounted Reset control and display Run/Hold selection.

The 6351A is a full Universal Counter Timer. In addition to those features outlined for the 6341A TIM and Ratio measurements are provided. Time interval single shot measurements with selectable resolution from 10 ns to 10 μs, and ratio measurements with input frequencies to 100 MHz on both channels. Full input conditioning trigger level and preset control, attenuation, slope selection and ac/dc coupling on both channels.

The 6361A is a Dual Universal Counter Timer providing a new concept in universal measurement. To fully understand and appreciate this instrument, we must first understand that it shares all the features of any universal counter timer. In fact that is where it started, a 100 MHz/10 ns TIM/PERIOD ac/dc coupled Universal Counter.

Next, both channels are identical, in characteristics and capability. This allows each channel to be used for both frequency measurements from dc to 100 MHz and period measurements with resolutions of 10 μs to 10 ns.

Because of this feature it is natural that both channels can be used simultaneously thus providing simultaneous measurements of two frequencies or two periods. To further enhance it's capabilities two digital displays are provided.

Dual simultaneous measurements bring forth the additional functions of Alternate Period. Conventional counters measure period of input events in an alternating method. This yields the period of every other event, assuming the input rate is slower than the recovery time. Due to it's dual capabilities the 6361A will display not only the conventional reading, but also those alternate periods missed by conventional counters, assuming an input rate $\leqslant$500 Hz. Another feature of this instrument is ratio capability. Because both A and B channels are identical, the ratio ranges are identical dc to 100 MHz, with complete input conditioning.

The combination of measurements and applications are endless. An operator may wish to measure the repetative rate of an input pulse train as well as it's pulse width. This is easily accomplished and because of it's dual features, simultaneous measurement of both frequency and period are made and displayed.

NOTE

On the 6361A Dual Units the two RESET pushbutton switches are interrelated in their functions, due to the use of a common time base for both A and B channels. When the RATE function is selected depressing the RESET pushbutton on that channel will also reset the other channel. When operating in any function other than RATE the depression of the RESET pushbutton will reset it's appropriate channel and close the count gate on the other channel for a period that the pushbutton is held in it's depressed position, thus causing an erroneous count to accrue. Whenever a RESET is initiated, disregard the readout of that measurement cycle and take a reading on the next measurement cycle.

TABLE 1-1 SPECIFICATIONS

Specifications are common to all models unless otherwise stated.

FREQUENCY MEASUREMENTS

Range:	dc to 100 MHz (dc); 10 Hz to 100 MHz (ac).
Resolution:	0.1 Hz to 100 Hz Selectable in decade steps.
Sensitivity:	10 mV rms, dc to 100 MHz.
Accuracy:	±1 Count ±Time base accuracy.
Inputs 6361A:	Channel A and/or B.
Inputs 6351A and 6341A:	Channel B.

PERIOD MEASUREMENTS

Range:	dc to 100 MHz.
Resolution:	10 ns to 10 μs Selectable in decade steps.
Sensitivity:	100 mV rms, 0 to 100 Hz. 50 mV rms, 100 Hz to 10 kHz. 30 mV rms, 10 kHz to 1 MHz. 10 mV rms, 1 MHz to 100 MHz.
Accuracy:	±1 Count ±Time base ±Trigger error.
Trigger Error:	$\frac{\pm 0.05\ \mu s}{\text{Signal Slope in V}/\mu s}$ ±30 ns
Frequency Counted:	100 MHz to 100 kHz in decade steps, a function of resolution selection.
Inputs 6361A:	Channel A and/or B.
Input 6351A and 6341A:	Channel B.

ALTERNATE PERIOD (6361A only)

Range:	dc to 100 MHz.
Resolution:	10 ns to 10 μs selectable in decade steps.
Sensitivity:	100 mV rms, 0 to 100 Hz. 50 mV rms, 100 Hz to 10 kHz. 30 mV rms, 10 kHz to 1 MHz. 10 mV rms, 1 MHz to 100 MHz.
Accuracy:	±1 Count ±Time base ±Trigger error.

TABLE 1-1 SPECIFICATIONS (CONT)

ALTERNATE PERIOD (6361A only) Con'd)

Trigger Error:	$\frac{\pm 0.05\ \mu s}{\text{Signal Slope in V}/\mu s}$ ±30 ns
Frequency Counted:	100 MHz to 100 kHz in decade steps, a function of resolution selection.
Input:	Channel A.
Display:	Even periods displayed on Channel A, odd periods on Channel B.
Maximum Input Rate:	Recovery time is such that in order to make a measurement on every period input the input must be ⩽ 500 Hz.

TIME INTERFAL MEASUREMENT
(6361A and 6351A only)

Range:	0.01 μs (10 ns) to 10^3 seconds.
Resolution:	10 ns to 10 μs selectable in decade steps.
Sensitivity:	100 mV rms, 0 to 100 Hz. 50 mV rms, 100 Hz to 10 kHz. 30 mV rms, 10 kHz to 1 MHz. 10 mV rms, 1 MHz to 100 MHz.
Accuracy:	±1 Couny ±Time base ±Trigger error.
Trigger Error:	$\frac{\pm 0.05\ \mu s}{\text{Signal Slope in V}/\mu s}$ ±30 ns
Frequency Counted:	100 MHz to 100 kHz in decade steps, a function of resolution selection.
Start Input:	Channel A.
Stop Input:	Channel B.

RATIO MEASUREMENT
(6361A and 6351A only)

Range:	Fa Input: dc to 100 MHz (dc); 10 Hz to 100 MHz (ac). Fb Input: dc to 100 MHz (dc); 10 Hz to 100 MHz (ac).
Sensitivity:	10 mV rms, dc to 100 MHz.

TABLE 1-1 SPECIFICATIONS (CONT)

RATIO MEASUREMENT
(6361A and 6351A only) Cont'd

Inputs:	Fa:	Channel A.
	Fb:	Channel B.
Display:	Fb/Fa.	

EXTERNAL TIME BASE RATIO

Range:	Rate Input:	1 kHz to 100 MHz.
	Ext. T.B.:	1 kHz to 10 MHz.
Inputs:	Rate Input:	Channel A or B.
	Ext. T.B.:	Rear Panel J1.

SIMULTANEOUS MEASUREMENT
(6361A only)

Description:	Due to the dual channel concept each channel may be used for independent or simultaneous measurement of frequency, period, time interval, and ratio.
Specifications:	Each mode retains the characteristics and functions as detailed in the aforementioned specifications.
Simultaneous Combinations:	The following table illustrates the measurements and display combinations for simultaneous measurements.

Channel A Display	Channel B Display
Frequency	Frequency
Frequency	Period
Frequency	TIM
Frequency	Ratio
Period	Frequency
Period	Period
Period	TIM
Period	Ratio
TIM	Frequency
TIM	Period
TIM	TIM
TIM	Ratio

STANDARD TIME BASE

Crystal Frequency:	10 MHz.
Stability:	See Oscillator Specifications.

TABLE 1-1 SPECIFICATIONS (CONT)

STANDARD TIME BASE Cont'd

External Time Base:	Accepts 1 kHz to 10 MHz via rear panel connector. INT/EXT switch selects T.B. source.
	For proper annunciator and decimal point display the external input must be 10 MHz.
External Time Base Characteristics:	Requires 1 Vrms into 500Ω dynamic ac coupled.

INPUT CHARACTERISTICS

Coupling:	Switch selectable ac or dc.	
Input Impedance:	1 MΩ 25 pF.	
Attentuation:	Switch selectable X1, X10 and X100.	
Maximum Input: (without damage)	X1 Atten:	dc to 500 kHz, 125 Vrms; 500 kHz to 5 MHz, 50 Vrms; 5 MHz to 100 MHz, 10 Vrms.
	X10 Atten:	dc to 500 kHz, 250 Vrms; 500 kHz to 5 MHz, 100 Vrms; 5 MHz to 100 MHz, 20 Vrms.
	X100 Atten:	dc to 500 kHz, 500 Vrms; 500 kHz to 5 MHz, 200 Vrms; 5 MHz to 100 MHz, 40 Vrms.
Trigger Level:	±0.5V (X atten.) adjustable; OV in preset position.	
Slope:	±Switch selectable.	

GENERAL

Display:	8 digits (6361A has two 8 digit displays) 0.4 inch LED's. No mercury. Leading zero suppression with automatically positioned decimal for direct readout in kHz.

TABLE 1-1 SPECIFICATIONS (CONT)

Display: (Cont)	ms or μs. kHz, ms, μs gate and Off Scale annunciators.
Display Storage:	Built-in storage provides continuous display of most recent measurement.
BCD Conversion:	Option 35. 1-2-4-8 coded, converts group serial outputs from the counter to standard BCD parallel format, including decimal and legend units. Two options required for 6361A.
Operating Temperature:	0°C to +50°C.
Power:	100/115 Vac or 200/230 Vac ±10%, 48 to 440 Hz, approximately 30 watts.
Dimensions:	5 1/4 H x 8 3/8 W x 13 1/2 D (13, 3 x 21, 3 x 34, 3 cm).
Weight:	15 lbs. (6, 8 kg) net max.; 22 lbs. (10 kg) shipping.

TABLE 1-2 ACCESSORIES

Part No.	Description
057567	For rack-mounting one instrument. Height is 7 inches and mount is a standard cabinet.
A10338	Coaxial cable, 6 ft., male BNC connector on each end.
J0622	"T" BNC connector.
RF0014	BNC terminator, 50-ohm.

TABLE 1-3 OSCILLATOR SPECIFICATIONS

	STANDARD	OPTION 08	OPTION 09	OPTION 10
Aging rate after warm-up	±2 parts in 10^6 per year	±1 part in 10^6 per year	±1 part in 10^6/year.	0.8 parts in 10^6/yr. after 60 days. 1 part in 10^8/day after 24 hours.
Frequency retrace for off periods to approx. 24 hrs.	—	±5 parts in 10^7 within 15 min.	±1 part in 10^7 within 15 minutes.	±3 parts in 10^8 after 4 hours. ±2 parts in 10^7 after 15 minutes.
Short term aging rate	5 parts in 10^9 rms for 1 sec. average	±5 parts in 10^8/day average for 3 days.	±1 part in 10^8/day average for 3 days.	5 parts in 10^{10} rms for 10 sec. average.
Temperature variation	±5 parts in 10^6 from 0 to +50°C.	TCXO ±1 part in 10^6 over 0 to +50°C.	TCXO ±5 parts in 10^7 over 0 to 50° C.	±1 part in 10^7 over 0 to 50°C.
±10% change in line voltage	±1 part in 10^7	±5 parts in 10^8	±1 part in 10^8	±3 parts in 10^9
Long term aging rate	±3 parts in 10^7 for 30 days	±3 parts in 10^7 for 30 days	±3 parts in 10^7 for 30 days	±1.5 parts in 10^7 for 30 days

CHAPTER 2

INSTALLATION

2.1 INTRODUCTION

The Model 63X1A Frequency Counter is shipped in operational condition and is ready for use as received. This chapter outlines the procedures for initial inspection and installation of the instrument. Instructions for reshipment are also included should the unit be returned to Systron-Donner Corporation for service or repair.

2.2 RECEIVING INSPECTION

Prior to accepting the counter from the shipper, inspect the condition of the shipping container for any indication of freight damage. Any sign of such damage must be noted by both the shipper and receiver and should be reported to the insurance investigator.

Immediately following removal of the instrument from the shipping carton, inspect for possible physical damage incurred during shipment. Check surfaces for scratches or dents and note condition of controls and connectors. Should any damage be noted, notify your nearest Systron-Donner representative - - - DO NOT USE THE COUNTER UNTIL INSTRUCTED TO DO SO BY THE REPRESENTATIVE.

2.3 RESHIPMENT

When the instrument is to be repackaged for shipment use the original packing materials. Your Systron-Donner field-office can provide materials similar to those used for the original factory packaging, or repackage the instrument following these general instructions.

General packaging instructions:

1) Attach a tag to the unit indicating the model number, serial number, name and address of the instrument owner, and a summary of the service or repairs required.

2) Wrap the instrument in heavy paper or plastic prior to placing it into the shipping container.

3) Select a strong carton or wooden box to house the instrument.

4) Use an adequate layer of shock-absorbing material on all sides of the instrument and protect the front panel with additional layers of cardboard. Be certain that there is no movement of the unit within the container.

5) Seal the package with strong tape of metal bands.

6) Mark the shipping container "FRAGILE-DELICATE INSTRUMENT" to ensure careful handling.

7) Be certain that all correspondence refers to full instrument nomenclature (model and serial number).

2.4 POWER REQUIREMENTS

The Model 63X1A Frequency Counter is supplied with a standard three-conductor power cord which when plugged into an appropriate power receptacle, grounds the unit to protect operating personnel from certain electrical hazards. Whenever the power cord is mated to a two-conductor outlet, a cord adapter plug (properly installed) will provide the same protection.

The instrument operates from an ac power source. On ac it operates from either 100, 115, 125, 215, 225, 230 or 240 volts at 48 to 400 Hz and consumes approximately 30 watts. The instrument is normally factory wired for 115 volt operation.

Prior to connecting the instrument to any other source (115 V ac), insure the transformer primary is properly connected. Refer to Figure 2-1 for complete wiring description.

The power transformer primary can be configured for seven different line voltages by connecting and jumpering the taps in the different configurations listed as follows:

Line Voltage	Jumper	Line Connection
100V ac	2-4 and 3-5	H to 2 N to 3
115V ac	1-4 and 3-5	H to 1 N to 3
125V ac	1-4 and 3-6	H to 1 N to 3
215V ac	3-4	H to 2 N to 5
225V ac	3-4	H to 2 N to 6
230V ac	3-4	H to 1 N to 5
240V ac	3-4	H to 1 N to 6

2.5 SYSTEM INTERFACE – OPTION 35

Interface to the BCD Module Assembly for conversion from group serial output data to parallel 1-2-4-8 BCD is provided for via the rear panel mounted 24 pin connector. Table 2-1 provides pin number and output signal coding information. Each channel is equipped with an output connector. The output data pin information is identical, therefore only one table is necessary.

TABLE 2-1 BCD OUT CONNECTOR

Pin	Description	Pin	Description
1	$\overline{Sb\ 10^7}$	13	DP 1 bit
2	$\overline{Sb\ 10^6}$	14	DP 2 bit
3	$\overline{Sb\ 10^5}$	15	DP 4 bit
4	$\overline{Sb\ 10^4}$	16	$\overline{EOC}$
5	$\overline{Sb\ 10^3}$	17	$\overline{RESET\ INHIBIT}$
6	$\overline{Sb\ 10^2}$	18	NC
7	$\overline{Sb\ 10^1}$	19	NC
8	$\overline{Sb\ 10^0}$	20	$\overline{kHz}$ (Annunciator)
9	1 bit	21	$\overline{\mu s}$ (Annunciator)
10	2 bit	22	$\overline{ms}$ (Annunciator)
11	4 bit	23	+5V Reference
12	8 bit	24	0V Reference (GND)

Notes:
Sb = Strobe data per decade
1 bit = binary 1-2-4-8 encoded data to convert group serial to parallel
DP = Decimal Point data
NC = Not connected

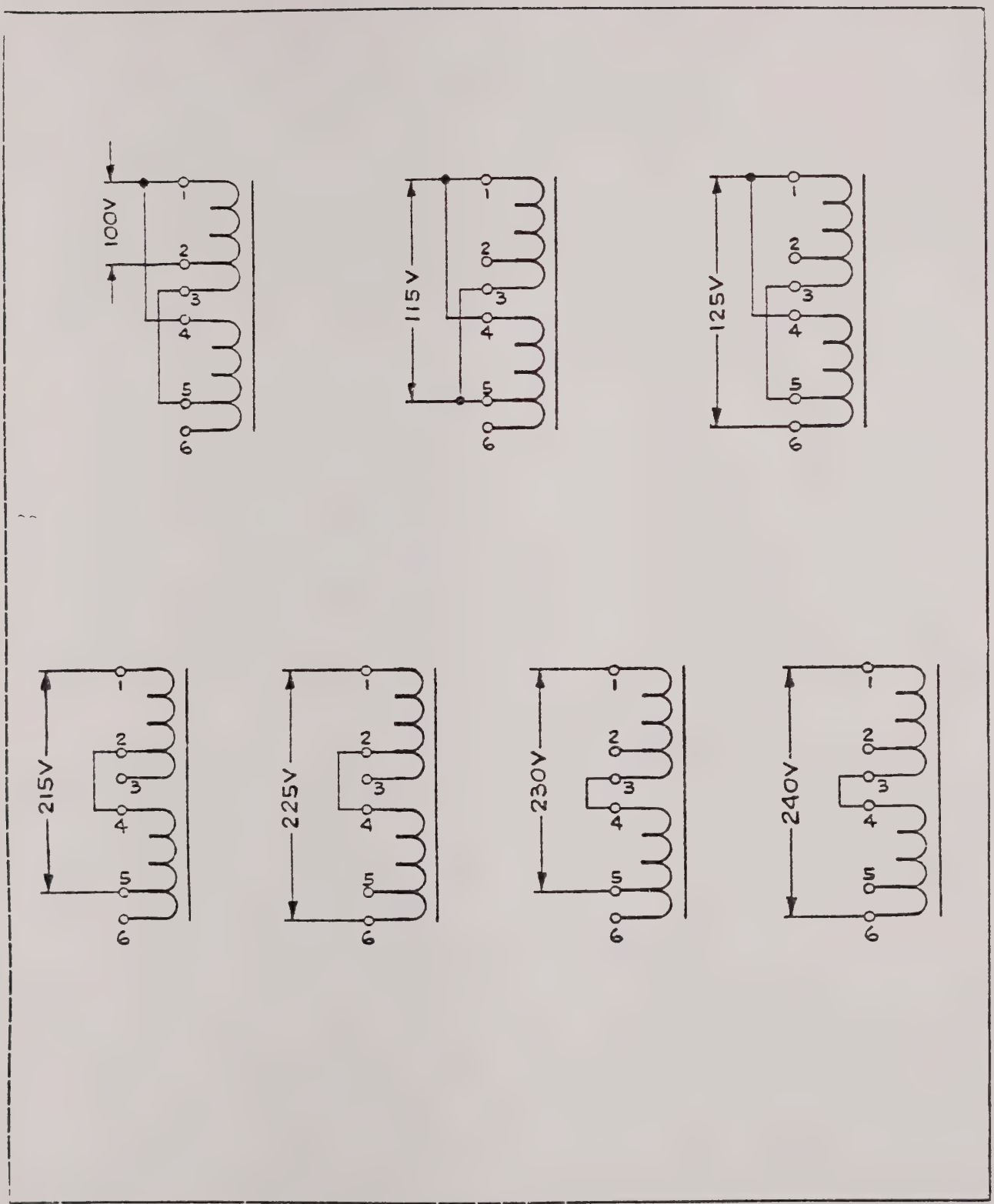


FIGURE 2-1
LINE CHANGE DIAGRAM POWER TRANSFORMER #05753201

CHAPTER 3

OPERATION

3.1 INTRODUCTION

Operation of the instrument is described in this chapter. A functional description of the front and rear panel controls connectors and indicators are provided. Turn on and the various typical measurement operations are also described in a step-by-step procedure.

The 63X1A Series Frequency Counters provide a group of counters covering the simple single channel counter to the more complex universal counter/timer with the added capability of simultaneous dual measurement function with corresponding dual digital display of these measurements. Operation will be described indicative of the function control and its related display. In those cases where the function and/or control and indication is similar regardless to unit, the function will be described only once. Table 3-1 describes the front panel and Table 3-2, the rear panel.

TABLE 3-1
FRONT PANEL CONTROLS AND INDICATORS

Nomenclature	Function
FUNCTION	Two section 6341A, or four section 6351A & 61A mode selector switches. Selects operating mode; Rate, Period, TIM A-B (time interval), Ratio B/A or Alternate Period. In RATE mode frequency measurement to 100 MHz are made (per channel) with resolution controlled by the Frequency Resolution switch. In PERIOD mode, period measurements 0 to 100 MHz (per channel) with selected resolution as controlled by Period Resolution switch. In TIM A-B mode, time interval measurements from 10 ns to 10^3 seconds are made. Start inputs are applied to the A channel and Stops to B channel. In RATIO B/A mode, B to A channel ratio measurements are made of input signals to 100 MHz per channel, with the appropriate ratio displayed on Channel B. In ALT PER mode, period measurements are made on each input pulse and displayed alternately first on the A channel display then on the B channel. The even number periods are read on the A display and the odd number periods on the B display. This function is available only on the A channel and will override the B channel function.
FREQUENCY RESOLUTION	Four section, resolution selector switches. Selects appropriate time base for 100 Hz, 10 Hz, 1 Hz or .1 Hz resolution of the input frequency when in the Rate mode and positions the decimal point on the display.
PERIOD/TIM RESOLUTION	Four section, resolution selector switches. Selects appropriate clock output from the time base for 10 ns to 10 μs, resolution in decade steps, of the period and or time interval measurement in process and positions the decimal point on the display.For period measurements only one input is employed per measurement selected. For TIM measurements starts are applied to the

TABLE 3-1 (CONT)
FRONT PANEL CONTROLS AND INDICATORS

	A channel and Stops to the B channel.
ATTENUATOR	Three selector switches (per channel), X1, X10, and X100. Part of the input conditioning circuits providing control over a variety of input levels and signals. Attenuates input signal amplitude by factors of 1, 10 or 100.
TRIGGER LEVEL	Potentiometer and switch. Determines exact point on the (Slope switch position) input waveform slope which will trigger the input circuits. Trigger level is continuously variable between -0.5V and +0.5V nominal times the attenuator switch setting. In the PRESET switch position input trigger level is at 0 volts nominal.
SLOPE +	Toggle switch. Determines which input waveform slope, (+) positive-going or (-) negative-going, will be used to trigger the input counting circuits.
DC/AC Switch	Toggle switch. Selects ac, dc coupling of the input signal. AC position couples the ac component of the input waveform to the counter. DC position couples the dc plus the ac components inputs to the counter.
INPUT	BNC connector per channel as appropriate. On the 6351A and 6361A, A and B channels have connectors. Used for inputting Rate A, Rate B, Period A, Period B, TIM A-B, B channel Ratio B/A and A channel Alternate Period.
RUN/HOLD	Toggle switch. Selects method of storing the displayed measurement. In the RUN setting the display is updated after each measurement cycle. In the HOLD setting only one measurement is made and the results held on the display (stored) indefinately. Pressing reset or switching to another mode will activate a single measurement cycle which will in turn be held indefinately.
RESET	Momentary push button switch. When depressed, resets the display and internal count circuits to zero and/or appropriate quiescent state. After finite reset period instrument begins new measurement cycle.
DIGITAL DISPLAY	Eight digit 0.4 inch seven segment LED readout with automatically positioned decimal point. Features leading zero suppression.
O.S.	Off Scale LED indicator illuminates when input exceeds the display capacity.
GATE	LED indicator, flashes to show the opening and closing of the time base gate.
kHz	LED indicator, illuminates when in the frequency mode. Provides direct readout in kHz of the frequency measured with resolution as determined by the Frequency Resolution switch and resulting decimal point location.
ms	LED indicator, illuminates when in the Period or TIM modes. Provides direct readout in ms of the period or TIM when in the 10 μs resolution setting of the Period/ TIM Resolution switches.

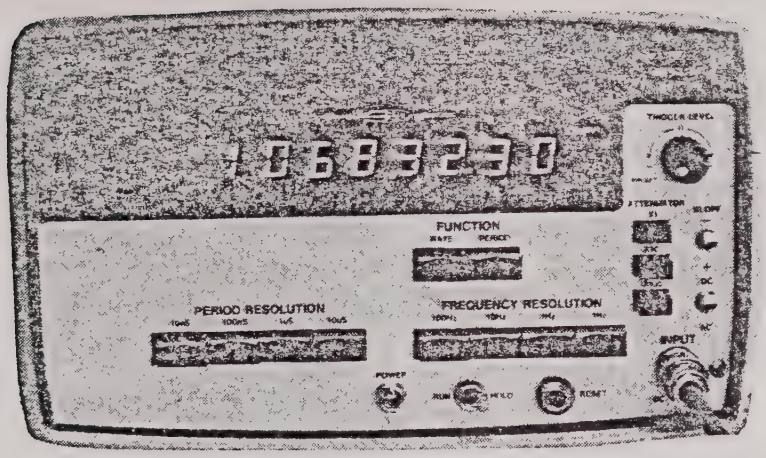


FIGURE 3-1 MODEL 6341A FRONT PANEL

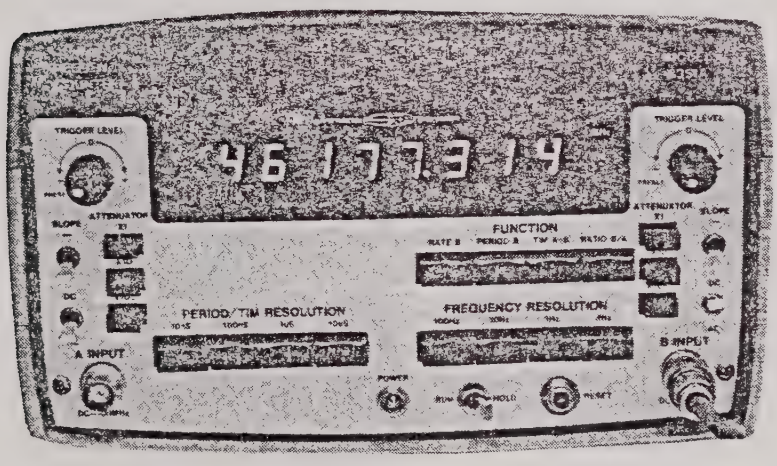


FIGURE 3-2 MODEL 6351A FRONT PANEL

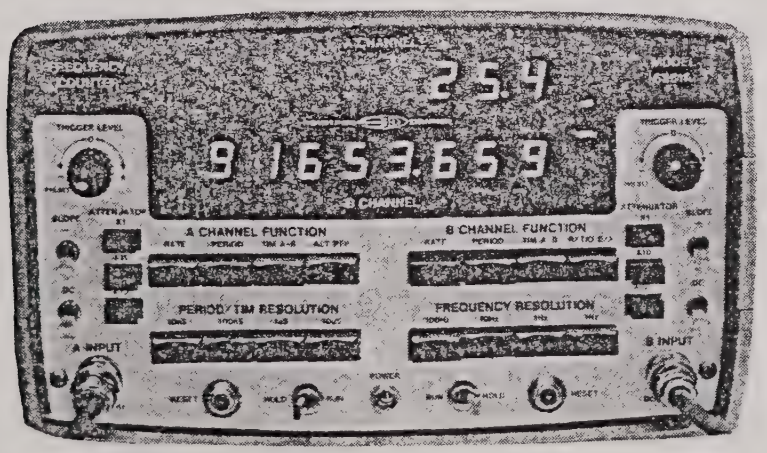


FIGURE 3-3 MODEL 6361A FRONT PANEL

TABLE 3-1 (CONT)
FRONT PANEL CONTROLS AND INDICATORS

μs ANNUNCIATOR	LED indicator, illuminates when in the Period or TIM modes. Provides direct readout in μs of the period or TIM when in the 10 ns, 100 ns or 1 μs resolution setting of the Period/TIM Resolution switches.
TRIGGER LEVEL INDICATOR	LED. Panel mounted indicator provides positive indication that input signal has triggered input amplifiers.

TABLE 3-2 REAR PANEL

Nomenclature	Function
B CHANNEL BCD OUT	24 pin connector. Option 35 BCD conversion interface connector.
A CHANNEL BCD OUT	24 pin connector. Option 35 BCD conversion interface connector.
INT/EXT SWITCH	Toggle switch. Selects time base reference oscillator. INT (internal) position selects the internal 10 MHz reference oscillator. In the EXT (external) position the internal oscillator is inhibited and the time base reference is derived from an external source.
10 MHz CLOCK IN	BNC connector. Accepts 1 kHz to 10 MHz, requires 1 Vrms, ac coupled into 500Ω. When used in conjunction with an external reference oscillator must be 10 MHz for proper decimal location and annunciator. When used as a Ratio input may be 1 kHz to 10 MHz.

TABLE 3-2 REAR PANEL (CONT)

10 MHz CLOCK OUT	BNC connector. Provides convenience output of the time base reference oscillator.
OSC ADJ	Access slot to time base oscillator adjustment.
FUSE HOLDER & POWER RECEPTACLE	Power connector and fuse holder 1A or .5A for 115 Vac or 230 Vac respectively.

3.2 MEASUREMENT CONSIDERATIONS

If the counter is to be used to make critical measurements, several factors, which can cause errors in the measurement results, must be considered. The following paragraphs will describe the significant error-producing factors, present practical solutions to these problems, and explain in detail (because of their effect upon measurement accuracy) the proper use of the input condition controls.

Accuracy of Measurements; Gating Ambiguity and Oscillator Stability.

Gating Ambiguity. The frequency counter, and most digital measureing instruments, is subject to an irreducible ±1 count error in the least significant digit of the display. This error is possible because the signal counted is not synchronized with the time base pulses that control the measurement gate.

The first or last cycle of the input signal may or may not pass into the count-chain during the selected measurement interval (gate). As the frequency measured is increased, the percentage of error, due to the ±count ambiguity, is reduced because it becomes less significant compared to the total count. In any case, the percentage of error is a function of the frequency (rate) measured and the number of pulses counted, i.e. the time base gate time selected. While normally insignificant at high frequencies, this error becomes

more important as the input frequency decreases. For this reason, the period measurement function is commonly selected to obtain the greatest accuracy when measuring low frequencies.

Internal Oscillator Stability. The gating precision and therefore the accuracy of the count, is dependant upon internal oscillator stability. The frequency counter oscillator is initially set to 5 parts in 10^9 of a frequency standard. The deviation of the frequency counters oscillator from this standard becomes a function of several factors, the most important of which is time. Due to inconsistencies within the frequency determining elements of the oscillator, an aging rate will be established and can be recorded. The frequency counters aging rates are specified in Table 1-1. Generally, the aging rate decreases with time (provided the counter is energized).

Oscillator stability is, additionally, a function of line voltage and temperature but, except for the time period immediately following calibration, their effect will be several orders of magnitude less than that of the aging rate and may be neglected. To achieve the greatest measurement accuracy, the following considerations apply:

a. Insure that the counter is connected to an appropriate power source.

b. Monitor or regulate the ac line voltage (source).

c. Calibrate the frequency counters oscillator consistent with the maximum allowable error.

d. Substitute, if deemed necessary, a more stable external oscillator (via EXT time base connector) for the standard internal oscillator.

Input Signal Noise. Period and time interval measurements are subject to a trigger time error caused by noise on the input signal. The total signal can be considered to be an ideal noise-free signal with a superimposed noise signal. The noise, added to the ideal signal, may trigger the channel before or after the selected instant for triggering. The maximum error, in time, for a given peak-to-peak noise voltage (Vn) and a given ideal signal slope (at the selected trigger level) is:

$$t(\text{sec}) = \frac{Vn \quad (\text{volts})}{\text{Slope} \quad (\text{volts/sec.})}$$

The maximum percentage of error (T is the actual period) is:

$$\text{Max. \% error} = \frac{t \times 100 \text{ (sec.)}}{T \text{ (sec.)}}$$

For a sinewave triggering at its zero cross-over point:

$$\text{Max \% error} = \frac{Vn \times 100 \text{ (volts)}}{V \text{ sinewave (volts)}}$$

These errors lengthen or shorten a period measurement.

On the 6361A Dual Units the two RESET pushbutton switches are interrelated in their functions, due to the use of a common time base for both A and B channels. When the RATE function is selected depressing the RESET pushbutton on that channel will also reset the other channel. When operating in any function other than RATE the depression of the RESET pushbutton will reset it's appropriate channel and close the count gate on the other channel for a period that the pushbutton is held in it's depressed position, thus causing an erroneous count to accrue. Whenever a RESET is initiated, disregard the readout of that measurement cycle and take a reading on the next measurement cycle.

3.3 INPUT CONDITIONING CONTROLS

Because unstable and inaccurate measurements are often the result of improper input conditioning control settings, which produce inconsistent triggering of the instruments signal processor circuits, and because the input conditioning controls extend the frequency counters input signal overload capabilities, these controls receive special attention in the following paragraphs. The information presented applied to both the A and B channel input controls because these controls are functional identical.

Input Coupling. The AC/DC toggle switch selects either ac or dc coupling of the input signal into the attenuator assembly from the front panel connector. The DC position couples both the ac and dc components to the attenuator while the AC position couples only the ac component.

DC coupling is normally employed for very slow signals or repetitive signals with varying duty cycles. AC coupling is selected for high frequency inputs and for singals that have combined ac plus high level dc components.

Attenuation. The ATTENUATOR switches provide attenuation (division) of the input waveform amplitude by the factors labeled on the switches X1 (no division), X10 and X100. Because the TRIGGER LEVEL controls adjustable range, referenced to the applied input waveform, is dependant upon the attenuator switch setting, an explanation of the function of either must include the other. The combined explanation follows concluding with important attenuator switch use considerations.

Trigger Level Adjustments. The level control is an integral part of the input amplifier and sets the trigger voltage point of that amplifier. An output pulse is generated each time the input wave form passes through the hysteresis range of the amplifier (hysteresis range is a small, fixed voltage range centered around the LEVEL setting-selected dc level at the amplifiers input). The amplifier input dc level can be shifted, by the LEVEL control, in either a positive or negative direction, which allows the operator to select a particular point on the input waveform as the point which will produce consistent triggering of the amplifier. Triggering will occur whenever the selected input waveform trigger point and its associated hysteresis range are crossed by the input waveform.

With the attenuator switch at X1, the level controls adjustable range is ±0.5 volts; that is, the level control (in conjunction with the slope selection) can select any point on an input waveform ($\leq$1V peak-to-peak), provided the waveform is ac coupled, to be the trigger point. If the input waveform, given the preceding conditions, were 5V peak-to-peak, the level control could not be adjusted so that any desired trigger point would pass through the hysteresis range. However, by setting the attenuator to X10, the input would be attenuated by a factor of ten which would reduce the waveform to .5V peak-to-peak at the trigger amplifier input. This attenuated input would fall within the ±0.5V range of the level control.

Slope Determination. The SLOPE switch selects which input waveform slope, positive-going or negative-going, the level control is to act upon. That is, if the slope switch is at "+", the level control will select a level on the positive-going slope of the input waveform which will trigger the frequency counter measurement circuits. The selected level on the slope determines and defines the trigger point. The selected trigger level hysteresis range must be crossed by the input waveform, which in turn will produce a consistent trigger amplifier output, before the slope circuits can act on the trigger amplifier output. The slope circuitry shapers produce complementary outputs, one of which is selected by the slope switch-controlled slope gates. In either slope position, the trigger point is time coincident with the positive-going edge of the slope gates output pulse.

Input Control Consideration. The purpose of each input waveform trigger channel (A and B) is to consistently produce a reliable trigger pulse output which has a positive-going edge that occurs at the same instant as the selected trigger point. This condition can be achieved only if the attenuator and level controls are properly adjusted. Before adjusting the input conditioning controls, attempt to visualize the input waveform parameters. The following factors should be considered prior to any attempt to measure an unknown input waveform:

a. If the input signal amplitude is unknown, measure the amplitude with an oscilloscope prior to connection to the instrument. If amplitude-measuring test equipment is not available, set the attenuator to X100.

b. If the attenuated input waveform is very small, the trigger voltage level becomes critical - it may be set too low or to high to produce a pulse.

c. If the attenuated to-be-measured voltage variations are superimposed on a dc level, they may not cross the trigger voltage range.

d. Modulation, or other attenuated input signal variations, is least likely to produce trigger failure when the trigger voltage is set midway between the input signal peaks.

e. Extraneous signals (noise or modulation) have the least effect on the time at which a trigger pulse occurs when the input amplifier is set to trigger on the steepest slope of the input waveform.

f. External attenuation of noisy input signals may reduce the effects of the noise.

g. Attenuating the input signal, in reference to the trigger amplifier input, reduces the slope at all points and shifts the ac component, if it rides on a dc level, nearer to ground potential.

3.4 OPERATING PROCEDURES

The frequency counter may be operated in any one of several modes and in respect to the dual counter in two modes simultaneously.

Instrument Self Test.
The following procedure performs an operational check on the instrument and may be used as a confidence check for maintenance purposes, incoming inspection, troubleshooting, etc. No special test equipment is required. However, appropriate cable to route the signal from the rear panel to 10 MHz output to the respective input is required along with a TEE connector and 50Ω terminators. Connect the frequency counter to the appropriate power source. Turn the instrument on and allow the time base oscillator time to stabilize. The Model 6361A dual counter will be described in detail, similar measurements i.e. Period, Rate. Ratio B/A TIM are identical on all units.

Channel	Function	Slope	Resolution	Gate	O.S.	Display	Legend
A and B	Rate	N/A	100 Hz	Blinks	Off	10000.0	kHz
A and B	Rate	N/A	10 Hz	Blinks	Off	10000.00	kHz
A and B	Rate	N/A	1 Hz	Blinks	Off	10000.000	kHz
A and B	Rate	N/A	.1 Hz	Blinks	On	0000.0000	kHz
A and B	Period	N/A	10 ns	Blinks	Off	0.10	μs
A and B	Period	N/A	100 ns	Blinks	Off	0.1	μs
A and B	Period	N/A	1 μs	Blinks	Off	0.	μs
A and B	Period	N/A	10 μs	Blinks	Off	0.00	ms
A and B	TIM	A- B-	10 ns	Blinks	Off	0.10	μs
A and B	TIM	A+ B-	10 ns	Blinks	Off	0.04	μs
A and B	TIM	A- B+	10 ns	Blinks	Off	0.06	μs
A and B	TIM	A- B-	100 ns	Blinks	Off	0.1	μs
A and B	TIM	A+B+	100 ns	Blinks	Off	0.1	μs
A and B	TIM	A+B+	1 μs	Blinks	Off	0.	μs
A and B	TIM	A+B+	10 μs	Blinks	Off	0.00	ms
B	Ratio B/A	N/A	N/A	Blinks	Off	1.	none
A	Alternate	N/A	10 ns	On	Off	0.10	μs
A	Alternate	N/A	100 ns	On	Off	0.1	μs
A	Alternate	N/A	1 μs	On	Off	0.	μs
A	Alternate	N/A	10 μs	On	Off	0.00	ms

NOTE: Alternate Period overrides the B Channel function.

Self Test Procedure.
1. Using TEE, 50Ω terminators and coax cables connect the 10 MHz Output to the A and B inputs and terminate both inputs at 50Ω.

2. Set the conditioning controls as follows: Trigger level to Preset. Attenuator to X1. AC/DC to AC.

3. Set the RUN/HOLD switch to RUN and observe the display as indicated in the following table for the appropriate Function/Resolution settings. All readings are ±1 count.

4. Set the RUN/HOLD switches to HOLD, the Function switches to Rate and Resolution to 1 Hz in that order. Observe that the legend and decimal point will shift, however, the display will not update, also the Gate lamp remains off.

5. Depress RESET. Observe that the instrument makes one measurement cycle (gate lamp blinks on then off and remains off) only. A new measurement is made only upon manual reset.

Functional Operating Procedures.
Step-by-step operating procedures for each of five distinct functions are presented.

Figures 3-1, 3-2 and 3-3 depict each of the counters. The operating procedure is applicable to all models. On the 6261A Dual Units Function Modes can be mixed.

Rate Function - Single and Dual Units.
1. Insure rear panel INT/EXT oscillator switch is set to INT, or if set to EXT input appropriate signal.

2. Set POWER to on (up).

3. Select appropriate Attenuator, Slope and AC/DC coupling.

4. Set RUN/HOLD to desired setting.

5. Depress RATE function switch per channel as appropriate.

6. Depress FREQUENCY RESOLUTION switch for desired resolution (time base) 100 Hz, 10 Hz, 1 Hz or .1 Hz.

7. Connect input signal to INPUT connector(s) as appropriate.

8. Adjust trigger level for stable reading on the display. If in HOLD depress RESET for each measurement.

9. Read measurement in kHz on the display. Leading zeros are blanked and the decimal point is automatically positioned.

Period Function - Single and Dual Units.
1. Insure rear panel INT/EXT oscillator switch is set to INT; or if set to EXT, input appropriate signal.

2. Set POWER to on (up).

3. Select appropriate Attenuator, Slope and AC/DC coupling.

4. Set RUN/HOLD to desired setting.

5. Depress PERIOD function switch per channel as appropriate.

6. Depress PERIOD/TIM RESOLUTION switch for desired resolution, 10 ns, 100 ns, 1 μs or 10 μs.

7. Connect input signal to INPUT connector(s) as appropriate.

8. Adjust appropriate TRIGGER LEVEL for stable reading on the display. If in HOLD depress RESET for each measurement.

9. Read measurement in ms or μs on the display. Leading zeros are blanked and the decimal point is positioned automatically.

TIM A-B Function - Single and Dual Units.
1. Insure rear panel INT/EXT oscillator switch is set to INT; or if set to EXT, input appropriate signal.

2. Set POWER to on (up).

3. Select appropriate Attenuator, Slope and AC/DC couplings.

4. Set RUN/HOLD to desired setting.

5. Depress TIM A-B Function switch per channel as appropriate.

6. Depress PERIOD/TIM RESOLUTION switch for desired resolution, 10 ns, 100 ns, 1 μs or 10 μs.

7. Connect Start Inputs to A channel and Stop Inputs B channel.

8. Adjust the respective Trigger Level controls to the desired Start and Stop trigger points. If in HOLD depress RESET for each measurement.

9. Read measurement in μs or ms on the display. Leading zeros are blanked and the decimal point is automatically positioned.

Ratio B/A Function - Single and Dual Units.

1. Set POWER switch to on (up).

2. Select appropriate Attenuator, Slope, and AC/DC couplings.

3. Set RUN/HOLD to desired setting.

4. Depress RATIO B/A function.

5. Connect inputs to the B and A input connectors.

6. Read ratio on the display.

External T.B. Ratio - Single and Dual Units.

Ratio is a function of Rate Input/Ext. T.B.

1. Set rear panel INT/EXT oscillator switch to EXT.

2. Set conditioning controls as appropriate.

3. Set RUN/HOLD to desired settings.

4. Depress RATE function switch.

5. Connect signal inputs to the INPUT connector and the rear panel EXT IN connector.
Range: input range 1 kHz to 100 MHz and EXT T.B. range 1 kHz to 10 MHz.

6. Read ratio on the display.

Alternate Period Function - Dual unit only.

1. Insure rear panel INT/EXT oscillator switch is set to INT; or if set to EXT, input appropriate signal.

2. Set POWER to on (up).

3. Select appropriate Attenuator, Slope and AC/DC coupling.

4. Set RUN/HOLD to desired setting.

5. Depress ALT PER function switch.

6. Depress PERIOD/TIM RESOLUTION switch for desired resolution, 10 ns, 100 ns, 1 μs or 10 μs.

7. Connect input signal to A INPUT.

8. Adjust TRIGGER LEVEL for stable reading on the display.

9. Read measurements on the A and B channel displays.

Reading is in μs or ms as a function of resolution with automatic decimal point location and leading zeros suppression. If in HOLD depress RESET for each measurement.

On the 6361A Dual Counter any of the above measurement functions can be combined for simultaneous measurements as controlled by the A and B Channel Functions. Ratio B/A and ALT PER obviously, are mutually exclusive. Also, obviously, when making similar functions on each channel, the resolution for either channel is a factor of the appropriate resolution control.

CHAPTER 4

PRINCIPLES OF OPERATION

4.1 INTRODUCTION

This chapter describes the principles of operation of the Model 63X1A Series Counters from three perspectives.

The physical configuration of the three counters and their relationship to model type is discussed first and is referenced to Figure 4-1, 63X1A Series Universal Assembly Subassemblies Location Diagram.

The overall functional operation is presented next and is referenced to Figure 4-3 Model 63X1A Series Counters Functional Schematic Diagram. This description covers the function select logic, the time base divider chain, the interface between the Mother Board and the A and B Decade Counter PCB Assemblies, the Display PCB Assembly and the 10 MHz Oscillator Assembly. Also the different configuration for the three counters is presented and detailed as to additions and deletions of circuits, controls and switches and the jumper wire configurations required for the model type differences.

And last, a detailed theory of operation of the 100 MHz Amplifier PCB Assembly, the Decade Counter PCB Assembly, the Display PCB Assembly and the 10 MHz Oscillator Assembly is presented. This detailed circuit analysis is referenced to the schematic diagrams located in Chapter 7 of the manual.

4.2 MODEL TYPE PHYSICAL CONFIGURATION

The 63X1A Series is comprised of three different counters that utilize a common Universal Assembly that consists of the Mother PCB Assembly, the Rear Panel Assembly, the Front Panel Assembly and the 10 MHz Oscillator Assembly.

Table 4-1 provides a listing of the subassemblies and their relationship to model configuration. Figure 4-1 provides identification as to the location of the subassemblies installed on the Universal Assembly.

TABLE 4-1 MODEL 63X1A SERIES CONFIGURATION

ASSEMBLY			
REF	NAME	SD PART NO.	MODEL(S)
	Universal Assy.	057831	6341A/6351A/ 6361A
	Front Panel Assy.	057832	
	Rear Panel Assy.	057736	
	Mother PCB Assy.	057401	
	10 MHz Oscillator Assy.	05708801	
A1	Display PCB Assy 6361A	0574501	6361A
A1	Display PCB Assy 6351A	0574502	6351A
A1	Display PCB Assy 6341A	0574503	6341A
A2	B Channel 100 MHz Amplifier Assy.	057720	6351A/6361A
A3	B Channel Decade Counter PCB Assy.	05745701	6351A/6361A
A4	A Channel 100 MHz Amplifier Assy.	057721	6341A/6351A/ 6361A
A5	A Channel Decade Counter PCB Assy.	05745701	6341A/6351A/ 6361A
	6341A Decorative Panel	057601	6341A
	6351A Decorative Panel	057602	6351A
	6361A Decorative Panel	057603	6361A

4.3 FUNCTIONAL OPERATION

Figure 4-2 Model 63X1A Series Counter Functional Schematic Diagram supports the following functional analysis and detailed description of the logic circuits located on the Mother PCB Assembly.

The resolution and function selector switches are located on the Display PCB Assembly A1 and interface with the select logic and time base circuits located on the Mother PCB Assembly.

4.3.1 Resolution Select Logic And Time Base Circuits

The Time Base is referenced to the internal 10 MHz Oscillator or an external 10 MHz reference. The time base reference source is selected via the rear panel INT-EXT selector switch S4 and the gate select logic comprised of Quad NAND gate U18. Two rear panel BNC connectors are provided; the 10 MHz CLOCK IN connector J1 accepts the external 10 MHz reference and applies it to gate U18 pin 1 via transistor Q3, and the 10 MHz CLOCK OUT connector J2 supplies a output of the selected 10 MHz time base reference via driver U18-8.

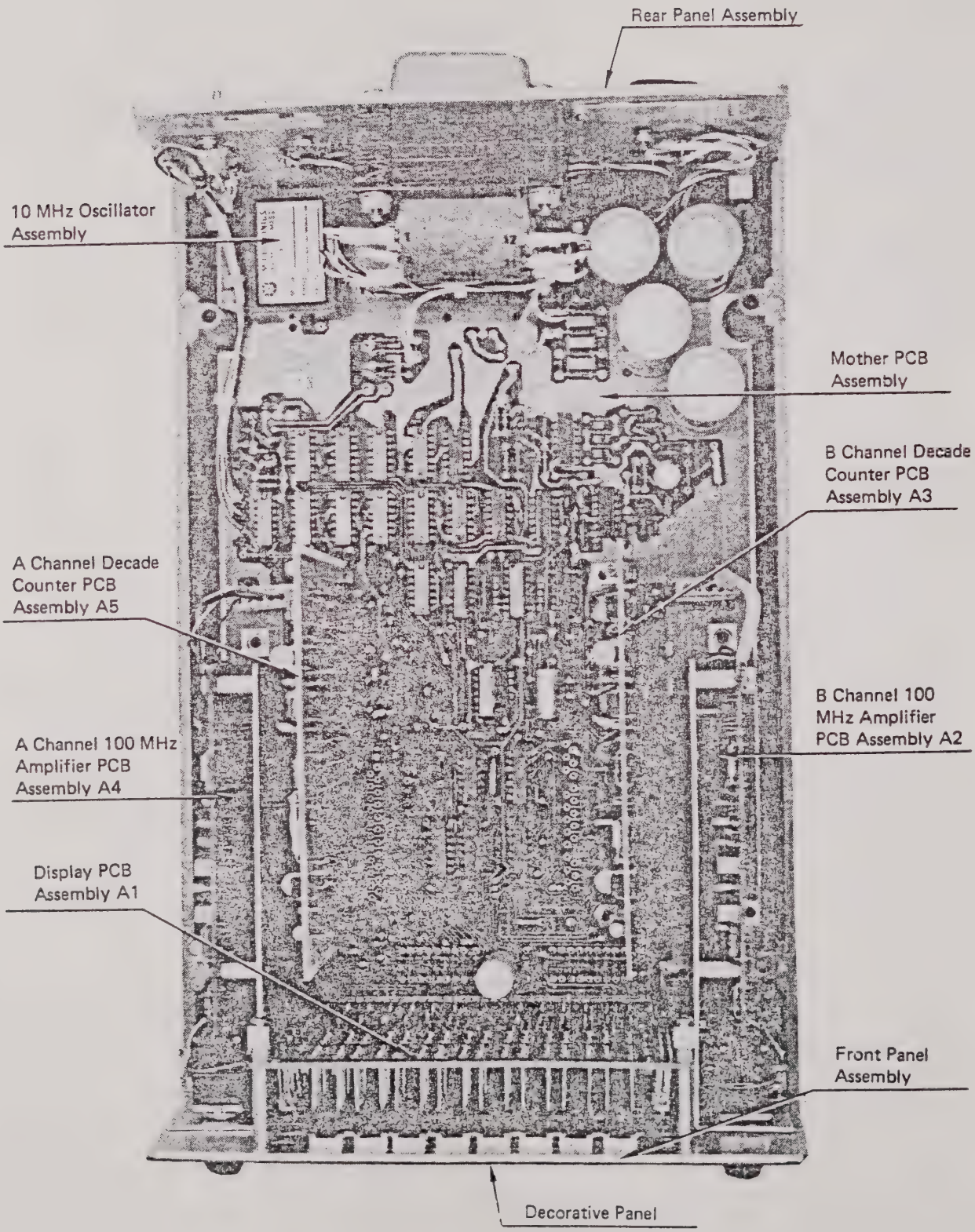

Rear Panel Assembly
10 MHz Oscillator Assembly
Mother PCB Assembly
B Channel Decade Counter PCB Assembly A3
A Channel Decade Counter PCB Assembly A5
B Channel 100 MHz Amplifier PCB Assembly A2
A Channel 100 MHz Amplifier PCB Assembly A4
Display PCB Assembly A1
Front Panel Assembly
Decorative Panel

FIGURE 4-1 63X1A SERIES ASSEMBLY LOCATION DIAGRAM

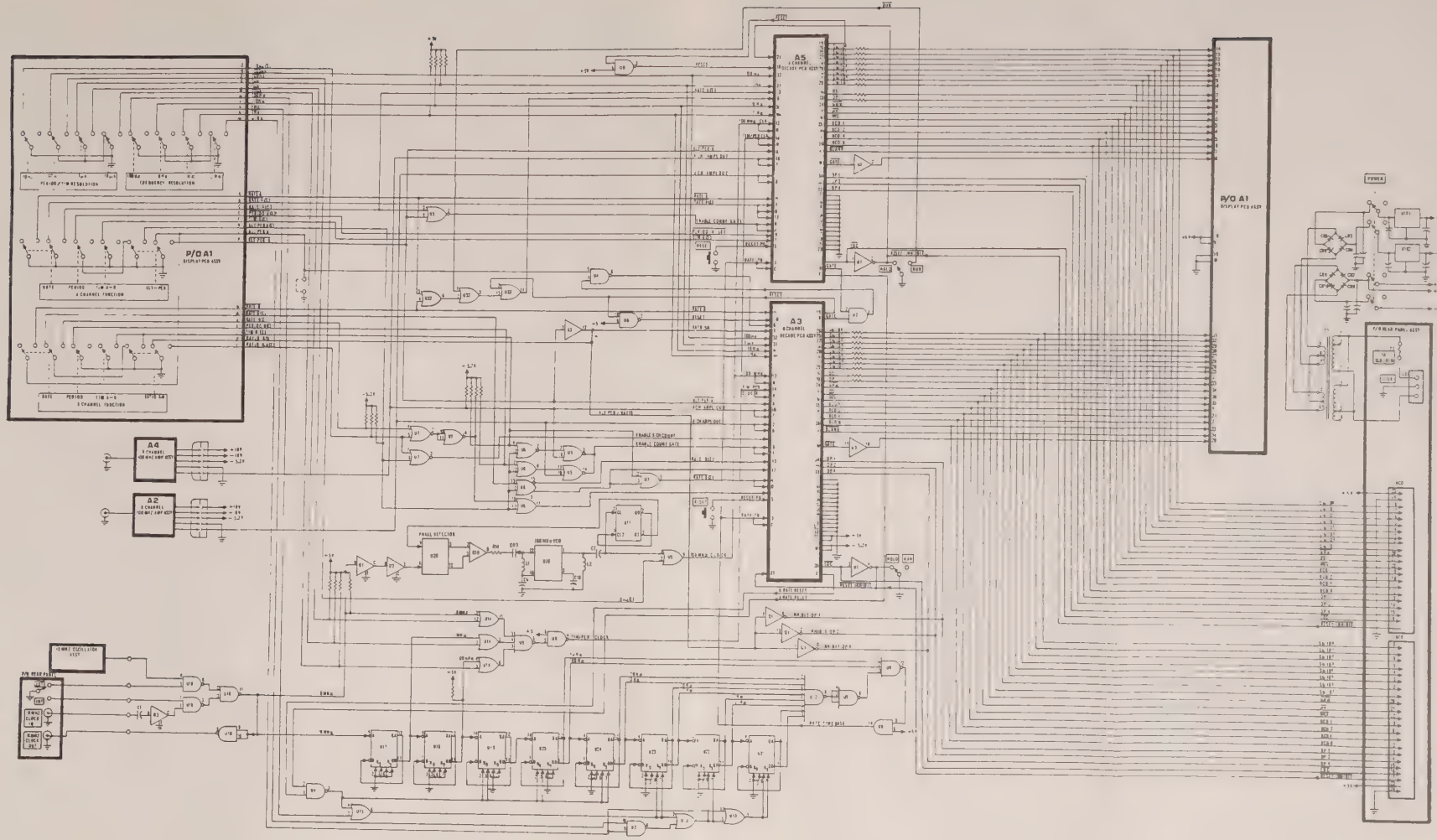


FIGURE 4-2
MODEL 63X1A SERIES COUNTER FUNCTIONAL SCHEMATIC DIAGRAM

The selected 10 MHz reference is then applied from gate U18 pin 11 as a TTL 10 MHz clock to the time base divider chain at U17 pin 14 and the 100 MHz phase locked oscillator circuit at the base of transistor Q1.

The Time Base Count Chain is configured by eight TTL ÷10 decade counters (U15 through U17 and U21 through U25). The RATE (FREQUENCY) resolution selection of the RATE TIME BASE is by the rate time base gate logic comprised of AND gate U2-8, NAND gate U4-3 and OR gates U13-6, U13-3 and U13-11. The six least significant decade counters are reset to the 009999 state with: an ALT/PER Function Selection, a manual RESET and when RATE A RESET (from A5-X) and RATE B RESET (from A3-X) are applied to NAND gate A4-3 coincident with EOC. When .1 Hz resolution is selected the decade counter U21 is preset to it's 9 state, when the 1 Hz resolution is selected decade counters U22 and U21 are preset to their 9 states, when 10 Hz resolution is selected decade counters U23, U22 and U21 are preset to their 9 states and when 100 Hz resolution is selected decade counters U24, U23, U22 and U21 are preset to their 9 states. The QA and QD outputs of decade counters U21 through U25 are combined by gates U9-8, U9-12 and U12-8 thus generating the selected RATE TB, which is applied to the TTL/ECL translator U8-14. Logic level translator U8-14 outputs the ECL RATE TB to the A and B Channel Decade PCB Assemblies RATE TB inputs at A5 and A3 pins 3 and C.

The PERIOD/TIM resolution is gate selected by OR gates U14-3, U14-6 and U14-11 and NAND gate U9-6 to generate the PER/TIM clock signals. When the 10 μs resolution is selected the 100 kHz clock from decade counter U16 pin 11 is enabled by gate U14-6. When the 1 μs resolution is selected the 1 MHz clock from decade counter U17 pin 11 is enabled by gate U14-3. And when the 100 ns resolution is selected the 10 MHz clock from NAND gate U18 pin 11 is enabled by gate U14-11. The selected 1 MHz, 10 MHz or 100 MHz clock is then applied to TTL/ECL translator U8-4. Logic level translator U8-4 outputs the ECL PER/TIM CLK to the A and B Channel Decade PCB Assemblies TIM CLK inputs at A5 and A3 pins 14 and R.

When the 10 ns resolution is selected ECL OR gate U5-9 is enabled which selects the 100 MHz clock from the 100 MHz PLL circuit output at capacitor C7 and applied it to the A and B Channel Decade PCB Assemblies 100 MHz inputs at A5 and A3 pins 12 and N. The 100 MHz Phase Lock Loop (PLL) circuit is comprised of Transistors Q1 and Q2, IC Phase-Frequency Detector U20, IC Differential Amplifier U19, IC Voltage Controlled Oscillator U10 (VCO) and U11 an ECL Bi-Quinary Counter that is configured as a ÷10 counter. The TTL 10 MHz clock from pin 11 of gate U18 is applied to the base of transistor Q1 which provides the TTL to ECL logic translation, this ECL 10 MHz clock is then emitter follower coupled by transistor Q2 to the reference (R) input of the phase detector at pin 6 of U20. The output of the ÷ 10 counter at U11 pin 2, its Q3 output, is applied to the variable (V) input pin 9 of phase detector U20. The phase detector outputs, the Up and Down signals at U20 pins 12 and 3 respectively which are applied to the integrating amplifier U19 and the resulting average level at U19 pin 6 is the phase difference error signal which is applied to the VCO's varicap CR3 to increase or decrease the VCO frequency and achieve phase lock of the 100 MHz VCO. The 100 MHz output of the VCO at U10 pin 1 is looped back via the ÷ 10 counter U11 as a 10 MHz clock to the variable (V) input of the phase detector U20 thus providing the PLL "feed back".

4.3.2 Function Select Interface

The A Channel and B Channel Function switches located on the Display PCB Assembly A1 interface via the Mother PCB with the A and B Channel Decade PCB Assemblies A5 and A3, and gate logic elements of the Mother PCB. Tables 4-2 and 4-3 provide a tabulation of the function interface.

TABLE 4-2
A CHANNEL FUNCTION SELECT INTERFACE

FUNCTION	FROM	TO
RATE A	A1-A	A5-n, U32-5
$\overline{\text{RATE A}}$ (ENABLE)	A1-B	A5-4, 17 and D
RATE A (ENABLE)	A1-C	A5-13, U5-5
$\overline{\text{PERIOD A}}$ (ENABLE)	A1-E	A5-V
$\overline{\text{TIM A}}$ (ENABLE)	A1-F	A5-1

TABLE 4-2 (Cont)
A CHANNEL FUNCTION SELECT INTERFACE

FUNCTION	FROM	TO
ALT PER A (ENABLE)	A1-N	U7-6, U6-12
ALT PER A	A1-c	U4-5, W1
$\overline{\text{ALT PER A}}$	A1-P	A3-A, A5-A and U3-13

TABLE 4-3
B CHANNEL FUNCTION SELECT INTERFACE

FUNCTION	FROM	TO
$\overline{\text{RATE B}}$	A1-b	U32-4, A3-n
$\overline{\text{RATE B}}$ (ENABLE)	A1-d	U6-13
RATE B (ENABLE)	A1-e	U7-4
$\overline{\text{PERIOD B}}$ (ENABLE)	A1-f	U6-7
TIM B (ENABLE)	A1-l	U6-4, U7-12
RATIO B/A	A1-p	U8-10, A3-19
RATIO B/A (ENABLE)	A1-r	U7-5, U7-7

Figure 4-3 illustrates the Function selection and signal routing in logic diagram format.

4.3.3 Power Supply Circuits

The power supply consists of the rear panel mounted power transformer T1, line Fuse F1, and the AC power input connector J3. The rectifiers, filter capacitors, four pole single throw POWER push-button switch and the +5V and -5.2V IC regulators are mounted on the Mother PCB Assembly.

The bridge rectifier consisting of diodes CR3 through CR6 supplies unregulated negative voltage to the -5.2 volt regulator U101 and positive unregulated voltage to the +5 volt regulator U102 via separate poles of the POWER push button switch. The bridge rectifier consisting of diodes CR7 through CR9 supplies unregulated +18V and -18V via separate poles of the POWER push button switch to the A and B 100 MHz Amplifier Assemblies A4 and A2. The A4 and A2 Assemblies have their own +15 volt and -15 volt IC regulators which are supplied by the +18V and -18V unregulated voltages from the Mother PCB rectifier.

When the Option 10 time base oscillator is installed, +18V from the rectifier is supplied directly to the oscillator whenever line voltage is applied to the counter.

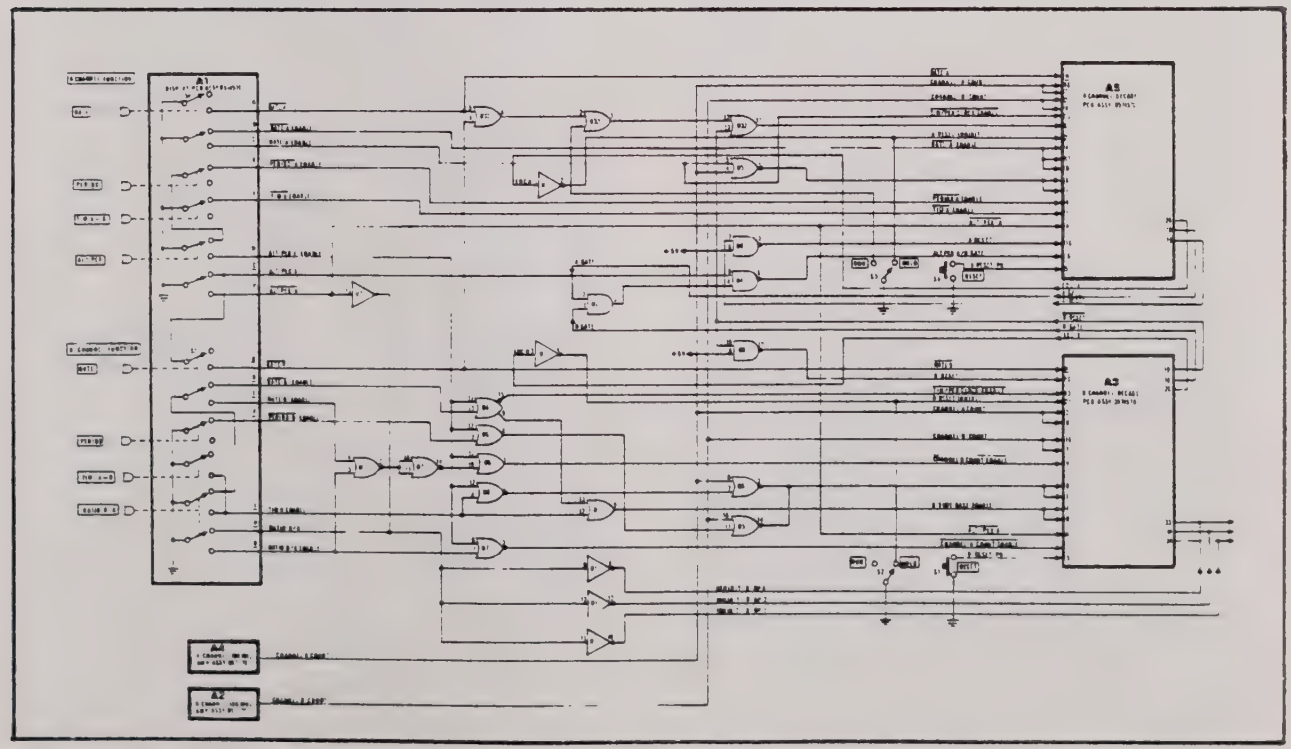


FIGURE 4-3 FUNCTION SELECTION LOGIC DIAGRAM

4.4 DISPLAY PCB ASSEMBLY A1

The following circuit description is referenced to Figure 7-11 Display PCB Assembly Schematic Diagram located in Chapter 7 of this manual.

The schematic diagram depicts the #0574501 assembly which is configured for the Model 6361A counter which utilizes a dual display and function switch configuration. When relating to the Model 6341A or 6351A refer to notes 2 and 3 of the schematic diagram for the deletion of the Channel A components, and switch elements, and the addition of the jumpers required for the Model 6341A or 6351A configuration, which are identified as A1 assemblies #05745703 and #05745702 respectively.

Since the A and B Channel display circuits are identical as to function and the only difference being the assigned reference designators, the detailed description will describe the B Channel display circuit only.

The B Channel display circuit consists of eight Seven Segment LED numerical display elements (DS1 through DS8), five LED indicators (DS9 through DS13) which provide the GATE, O.S. (Over Scale) and three units of measurement (μs, ms and kHz) indications. A SN74274N IC BCD-to-Seven-Segment Decoder/Driver and ten Darlington transistors (Q1 through Q10) for display illumination drive complete the Channel B display related components.

The B Channel display circuit receives multiplexed eight decade display data in a 1-2-4-8 BCD format which is applied to the BCD-to-Seven Segment Decoder/Driver (U1). Eight sequenced decade ground return strobes ($\overline{Sb\ 10^0}$ through $\overline{Sb\ 10^7}$) are applied to the eight P-N-P Darlington transistors (Q1 through Q8) in a descending order from 10^7 to 10^0 to illuminate the LED numerical display element in a sequential manner.

If the count displayed exceeds 99999999 a logic high will be generated and applied via A1 pin X, which will illuminate the O.S. LED indicator (DS-13) via N-P-N Darlington transistor Q10.

The $\overline{BLANK}$ signal applied to A1 pin 34 provides leading zero suppression of the numerical display and is applied to U1 pin 5 in proper sequential timing.

A decimal point (D.P.) sequential timed signal input at A1 pin 33 is applied via Darlington N-P-N transistor Q9 to pin 9 of each of the eight numerical display elements thus providing the proper decimal point location on the display.

The GATE and the three units of measurement LED's are illuminated on the presence of a TTL logic low being set on their appropriate A1 Connector pins.

4.5 DECADE PCB ASSEMBLIES A3 AND A5

The following circuit description is referenced to Figure 7-17 Decade PCB Assembly Schematic Diagram located in Chapter 7 of this manual and Figure 4-4 Decade PCB Assembly Functional Logic Diagram which accompanies the following circuit analysis.

4.5.1 Count Gate Logic

The Count Gate Logic consists of the select and enable gates U3, the count gate control flip-flops U6 which control the opening and closing of the count gate U9. The Count Gate Logic provides the mode selection of the RATE, PERIOD or TIM operation of the counter when interfaced with external logic located on the Mother PCB Assembly and the FUNCTION switch(es) located on the Display PCB Assembly.

The Count Gate, it's control logic and the 1st DCU Counter are configured from ECL integrated circuits to allow counting rates of up to 100 MHz.

When the RATE function is selected a logic low is set on U3 pins 11 and 12 which enables the RATE TB signal to the CE inputs of the count gate control flip-flops (U6 pins 6 and 11). Which inturn will open the Count Gate for a period of time set by the FREQUENCY RESOLUTION switch.

A logic low $\overline{RATE}$ enable is also set on the count

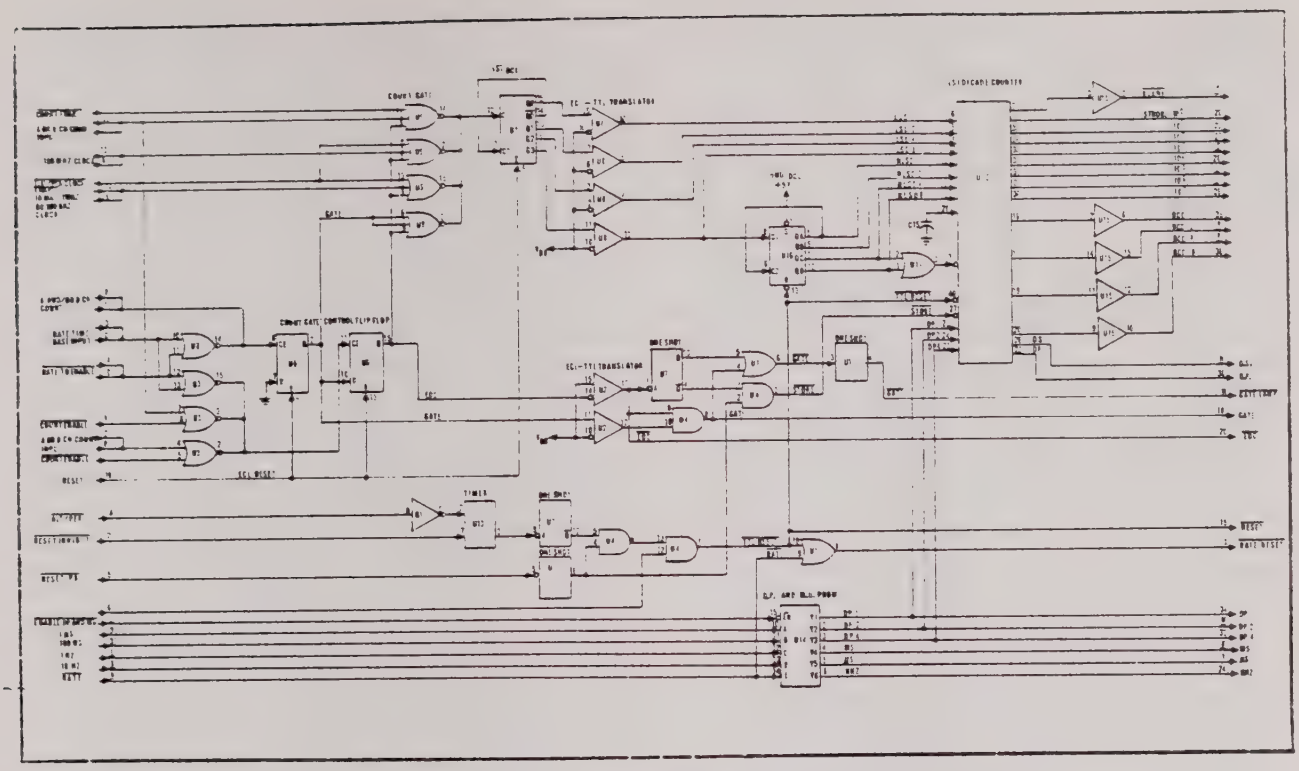


FIGURE 4-4
DECADE PCB ASSEMBLY FUNCTIONAL LOGIC DIAGRAM

gate U9 pin 11 to enable the count signal and allow it to be counted thus providing a rate (frequency) measurement.

When the PERIOD function is selected a logic low enable is set on U3 pin 6 which enables the input count signal to the CE input of the stop flip-flop (U6 pin 11). Also the input count signal from PCB pins 8 and J is enabled by external logic and applied to the CE input of the start flip-flop (U6 pin 6), which will open the count gate for the period measurement. A logic low $\overline{\text{PERIOD}}$ enable is also set on pins 4 and 13 of the count gate U9 to enable the selected clock frequency (PERIOD CLOCK) and allow it's accumulation by the counter, thus providing a period measurement.

When the TIM function is selected a logic low is set on U3 pin 5 as a $\overline{\text{TIM}}$ enable for the stop channel count applied to U3 pin 4. The start channel count is applied via pins 8 and J of the PCB to U6 pin 6 of the start flip-flop, thus allowing the count gate to open on the start signal and close on the stop signal. A logic low $\overline{\text{TIM}}$ enable is also set on pins 4 and 13 of the count gate U9 to enable the selected clock frequency (TIM CLOCK) and allow it's accumulation by the counter, thus providing a TIM measurement.

4.5.2 Counter Circuits

The selected and gated serial count from the Count Gate U9 is applied to the 1st DCU ECL Counter U5 pin 12 it's C1 input. The 1st DCU Counter outputs a 1-2-4-8 BCD count which is translated from ECL to TTL logic levels by the Quad Translator U8. ECL to TTL Translator U8 outputs the TTL BCD to the LSD BCD inputs of the 40-pin LSI Decade Counter U12 (pins 6, 5, 4, and 3). The LSD bit 8 is applied to the 2nd DCU TTL Counter U10 at it's C1 input pin 8. Counter U10 outputs a 1-2-4-8 BCD count to the NLSD BCD inputs of the 40-pin LSI Decade Counter U12 (pins 10, 11, 12 and 13). The NLSD bits 4 and 8 are gated by OR gate U11-3 to generate the NSLD $\overline{\text{CARRY}}$ signal which is applied to U12 pin 7 the $\overline{\text{CLOCK IN}}$ input.

The LSI Decade Counter U12 is controlled as to it's Count-Store-Reset cycle by the $\overline{\text{STORE}}$ signal

applied to pin 27 and the $\overline{\text{RESET}}$ pulse applied to pin 40. A 1-2-4 octal decimal point (D.P.) input is applied to U6 pins 25, 24 and 23 from the D.P. and M.U. ROM U14 to activate the Decade Counter's decimal point and leading zero suppression internal circuits.

The Decade Counter U12 outputs multiplexed eight decade display data in a 1-2-4-8 BCD format (pins 16, 17, 19 and 20) via four Buffer Drivers U15-6, 15, 12 and 10 to the Display PCB Assembly A1. The multiplexing frequency is determined by timing capacitor C15, which is connected between ground and pin 28 of U12 to control the frequency of U12's internal free-running M.V.

An eight line sequenced return to ground decade enable strobes, timed to illuminate the LED numerical display, is applied to the Display PCB Assembly A1 via the Decade PCB edge connector, pins 26, 25, 27, d, 28, e, f, and 29. These strobes are sequenced in descending order from decade 10^7 to 10^0.

When the Decade Counter U12 exceeds a count of 99999999 a logic high is generated at U12 pin 26 as the O.S. (over scale) signal, which will illuminate the Display LED indicator via the Decade PCB connector pin h.

4.5.3 Measurement Unit And Decimal Point Incoder

The incoding of the resolution selection into decimal point (D.P.) and unit of measurement (M.U.) data is provided by ROM U14. U14 is type 74188A 256-bit programmable read-only memory (PROM) which has been programmed to provide the D.P. and M.U. incoding functions. When programmed for the 63X1A series counters it's assigned a SD 07306 part number. Table 4-4 provides a "Truth Table" of the U14 incode program.

The ROM U14 outputs Y1, Y2 and Y3 (pins 1, 2 and 3) provides a 1-2-4 octal code to the Decade Counter U12 D.P. inputs at pins 25, 24 and 23. It's Y4, Y5 and Y6 outputs (U14 pins 4, 5 and 6) provides the unit of measurement data in ms, μs and kHz respectively to the Display PCB Assembly A1.

TABLE 4-4 U14 ROM PROGRAM (TRUTH TABLE)

ROM INPUTS						ROM OUTPUTS						Resolution Selected
A	B	C	D	E	EN	Y1	Y2	Y3	Y4	Y5	Y6	
0	0	0	0	0	0	1	0	0	1	1	0	100 Hz
0	0	0	1	0	0	0	1	0	1	1	0	10 Hz
0	0	1	0	0	0	1	1	0	1	1	0	1 Hz
0	0	1	1	0	0	0	0	1	1	1	0	.1 Hz
0	1	0	0	0	0	1	0	0	1	1	0	100 Hz
0	1	0	1	0	0	0	1	0	1	1	0	10 Hz
0	1	1	0	0	0	1	1	0	1	1	0	1 Hz
0	1	1	1	0	0	0	0	1	1	1	0	.1 Hz
1	0	0	0	0	0	1	0	0	1	1	0	100 Hz
1	0	0	1	0	0	0	1	0	1	1	0	10 Hz
1	0	1	0	0	0	1	1	0	1	1	0	1 Hz
1	0	1	1	0	0	0	0	1	1	1	0	.1 Hz
1	1	0	0	0	0	1	0	0	1	1	0	100 Hz
1	1	0	1	0	0	0	1	0	1	1	0	10 Hz
1	1	1	0	0	0	1	1	0	1	1	0	1 Hz
1	1	1	1	0	0	0	0	1	1	1	0	.1 Hz
0	0	0	0	1	0	0	1	0	1	0	1	10 ns
0	1	0	0	1	0	1	0	0	1	0	1	100 ns
1	0	0	0	1	0	0	0	0	1	0	1	1 μs
1	1	0	0	1	0	0	1	0	0	1	1	10 μs
0	0	0	1	1	0	0	1	0	1	0	1	10 ns
0	1	0	1	1	0	1	0	0	1	0	1	100 ns
1	0	0	1	1	0	0	0	0	1	0	1	1 μs
1	1	0	1	1	0	0	1	0	0	1	1	10 μs
0	0	1	0	1	0	0	1	0	1	0	1	10 ns
0	1	1	0	1	0	1	0	0	1	0	1	100 ns
1	0	1	0	1	0	0	0	0	1	0	1	1 μs
1	1	1	0	1	0	0	1	0	0	1	1	10 μs
0	0	1	1	1	0	0	1	0	1	0	1	10 ns
0	1	1	1	1	0	1	0	0	1	0	1	100 ns
1	0	1	1	1	0	0	0	0	1	0	1	1 μs
1	1	1	1	1	0	0	1	0	0	1	1	10 μs

4.5.4 Reset-Store Logic

The Reset-Store Logic generates the $\overline{\text{STORE}}$ and $\overline{\text{TTL RESET}}$ signals. The EOC signal from flip-flop U6 pin 15 is applied to pin 14 of ECL to TTL translator U2 which inverts and translates it to a TTL $\overline{\text{EOC}}$ signal. The $\overline{\text{EOC}}$ is then applied to the A input (pin 1) of the store one-shot M.V. U7 which generates the $\overline{\text{STORE}}$ signal at it's $\overline{\text{Q}}$ output pin 4 $\approx$ 10 μs after EOC. The $\overline{\text{STORE}}$ signal is then applied via AND gate U4-3 to the $\overline{\text{STORE}}$ input of the Decade Counter (U12 pin 27).

An EOC signal generated by external logic located on the Mother PCB Assembly is applied to the

Decade PCB Assembly connector pin 21, which will trigger the reset timer IC U13. Reset timer U13 will generate a logic high on it's output (U13 pin) ≈2 seconds after EOC time and trigger the reset one-shot M.V. U7 at it's A input pin 9. The reset one-shot M.V. $\overline{Q}$ output at U7 pin 12 is applied to pin 5 of AND gate U4 which will generate a logic high reset at it's output pin 6, on either a reset timer input (pin 5) or a reset P.B. input (pin 4). The reset at U4 pin 6 is then applied to AND gate input pin 13 of U4 where it is "OR"ed with a reset from the alternate channel applied to it's pin 12 via Decade PCB connector pin 6. U4 pin 11 outputs the $\overline{\text{TTL RESET}}$ to the 2nd DCU $\overline{\text{RESET}}$ (U10 pin 13), the Decade Counter $\overline{\text{RESET}}$ (U12 pin 40) and the Decade PCB connector pin 19. The $\overline{\text{TTL RESET}}$ at PCB connector pin 19 is translated by external logic located on the Mother PCB Assembly to an ECL RESET which is applied to PCB connector pin 10 to reset the count gate control flip-flops U6 and the 1st DCU counter U5.

4.6 100 MHz AMPLIFIER ASSEMBLIES A4 AND A2

The following circuit description is referenced to Figure 7-13 100 MHz Amplifier Assembly Schematic Diagram located in Chapter 7 of this manual.

The 100 MHz Amplifier Assembly contains a dc to 100 MHz wide band amplifier and associated controls that provides front panel configuration of it's operation for input signal conditioning. Front panel controls provide for the selection of input attenuation, ac-dc input coupling selection, triggering level adjustment, and + or – slope selection. A LED triggering indicator is also provided to aid in the proper setting of the triggering level.

The signal to be measured is applied to the INPUT DC – 100 MHz BNC connector J1 and coupled by capacitor C1 or directly to the input attenuator circuit via switch S1. The DC – AC toggel switch S1 provides for the selection of capacitor (ac) or direct (dc) coupling of the input signal.

The attenuator circuit is comprised of two divide by ten frequency compensated RC voltage dividers, which are switched in or out by the interlocked three element push button switch S2. When X1 attenuation is selected the signal is coupled directly to the FET input amplifier and no attenuation is inserted. When X10 attenuation is selected, one of the X10 dividers is inserted and when X100 attenuation is selected both X10 dividers are inserted in series, thus providing the selected attenuation factor.

The signal is coupled from the attenuator circuit to the A gate input of the dual FET input amplifier Q1 by RC frequency compensator C6 and R8. Diodes CR1 through CR4 provides the front end overload protection. The input amplifier circuit consisting of dual FET Q1, transistor array U3 and transistors Q2 and Q3 provides a high impedance (≥1 MΩ/25 pF) low noise signal – ended input. to a low impedance, differential output of sufficient amplitude to drive the ECL amplifier chain comprised of U2. The B gate of the input FET Q1 is connected to TRIGGER LEVEL control consisting of potentiometer R101 and switch S3. When the TRIGGER LEVEL control is placed in it's PRESET position Q1 FET B gate is set at ground and a zero volt triggering level is configured. When the TRIGGER LEVEL control is rotated, CW off of it's PRESET dedent, switch S3 removes the ground from the FET gate and connects it to the swinger of potentiometer R101 to provide an adjustable triggering level of –.5 volts - to - +.5 volts. The dual FET Q1 outputs as a source follower and it's sources are coupled via transistor array U3 and transistors Q3 and Q4 to the inputs of the ECL differential amplifier chain U2 pins 12 and 13. Transistor array U3 also provides the current source for FET Q1 which is configured with a Balance adjustment (R20) and a Bias adjustment (R19) to allow for the adjustment of the amplifiers sensitivity and zero balance.

The ECL three stage differential amplifier chain configured from U2 outputs it's differential signals at U2 pins 2 and 3 to the slope select gate logic. When the SLOPE switch S4 is placed in it's + position a ECL logic high is set on pin 4 of gate U1 and the true (positive slope) signal from U2 pin 3 is selected as the output signal at U1 pin 2. When the SLOPE switch is placed in it's – position a ECL logic high is set on pin 6 of gate U1 and the complement (negative slope) signal from U2 pin 2 is selected as the output signal at U1 pin 3.

The Trigger indicator LED CR101 is provided to aid in the proper setting of the TRIGGER LEVEL control. The complementry output of the differential amplifier at U2 pin 2 is inverted by gate U1-14 and applied to the M.V. configured by transistors Q4 and Q5. When the trigger level is properly adjusted the M.V. will free-run causing the LED CR101 to blink. When the trigger level is adjusted below it's proper triggering point transistor Q4 will turn on and prevent the M.V. from free running and extinguish the LED indicator. When the trigger level is set too high Q4 will be biased off and Q5 will turn on thus illuminating the LED.

CHAPTER 5

MAINTENANCE AND CALIBRATION

5.1 INTRODUCTION

This chapter provides information on the Performance Tests, Preliminary Maintenance and Calibration procedures for the 63X1A Series Frequency Counters. The IC's used in the 63X1A Series counters are listed and described as to their characteristics by the IC Data Sheets which provide pinning information, schematic equivalents and detailed characteristics that are unique to the IC device.

5.2 TEST AND CALIBRATION EQUIPMENT

Table 5-1 lists the test equipment required to perform the various procedures outlined in this Chapter.

TABLE 5-1
RECOMMENDED TEST EQUIPMENT

Oscilloscope Tektronix Model 465	100 MHz at 5 mV/cm Dual-Trace 5 ns/Div sweep rate.
Frequency Standard Hewlett Packard Model HP 105 A/B	1 MHz $<1 \times 10^{-10}$ short term stability.
Sweep Generator Wavetek Model 2001	0 - 200 MHz -33 dBm to +1 dBm output level
Digital Multimeter Systron-Donner Model 7004	ac and dc voltage ±.01% 4 Digit Display.

5.3 TIMEBASE OSCILLATOR CALIBRATION PROCEDURE

The accuracy of measurement is related to the stability of the time base reference oscillator. The calibration period for the reference oscillator is determined by two factors; the required measurement accuracy and the reference oscillators stability and aging rate. Figure 5.1 is a chart that will allow the service technician to determine the required calibration period. To find the required calibration period, lay a straight edge across the chart from the required measurement accuracy (left hand scale) to the reference oscillator stability (center scale), then read the calibration period off the right hand scale.

Four different reference oscillators may be installed in the counter, which have different aging rates and temperature stability specifications. Check the reference oscillator to determine if it is the standard or one of the optional oscillators, then check page 1-4 of this manual to find it's stability specification.

It is recommended that the following calibration be performed at an ambient temperature of +20°C (+68°F). To calibrate the reference oscillator use a 1 MHz Frequency Standard with an accuracy of at least 10 times the short term stability of the reference oscillator and an oscilloscope having a sweep rate of 0.01 μs/cm.

1. Apply the 1 MHz output of the Frequency Standard to the external trigger connector of the oscilloscope and set the sweep rate to 0.01 μs/cm and select the external trigger mode.

2. Place the counters rear panel INT/EXT toggle switch in it's INT position and connect the counters rear panel 10 MHz CLOCK OUT BNC connector to the vertical input of the oscilloscope.

3. Adjust the reference oscillator via the OSC ADJ rear panel access slot, for a near stationary waveform on the oscilloscope, then readjust after temperature stabilization is obtained for minimum drift of the waveform.

4. Monitor the oscilloscope noting the rate of drift. The amount of error as referenced to the Frequency Standard can be calculated by the drift rate. A 1 cm/s drift rate indicates an error of 1 part in 10^{-8} (0.01 PPM).

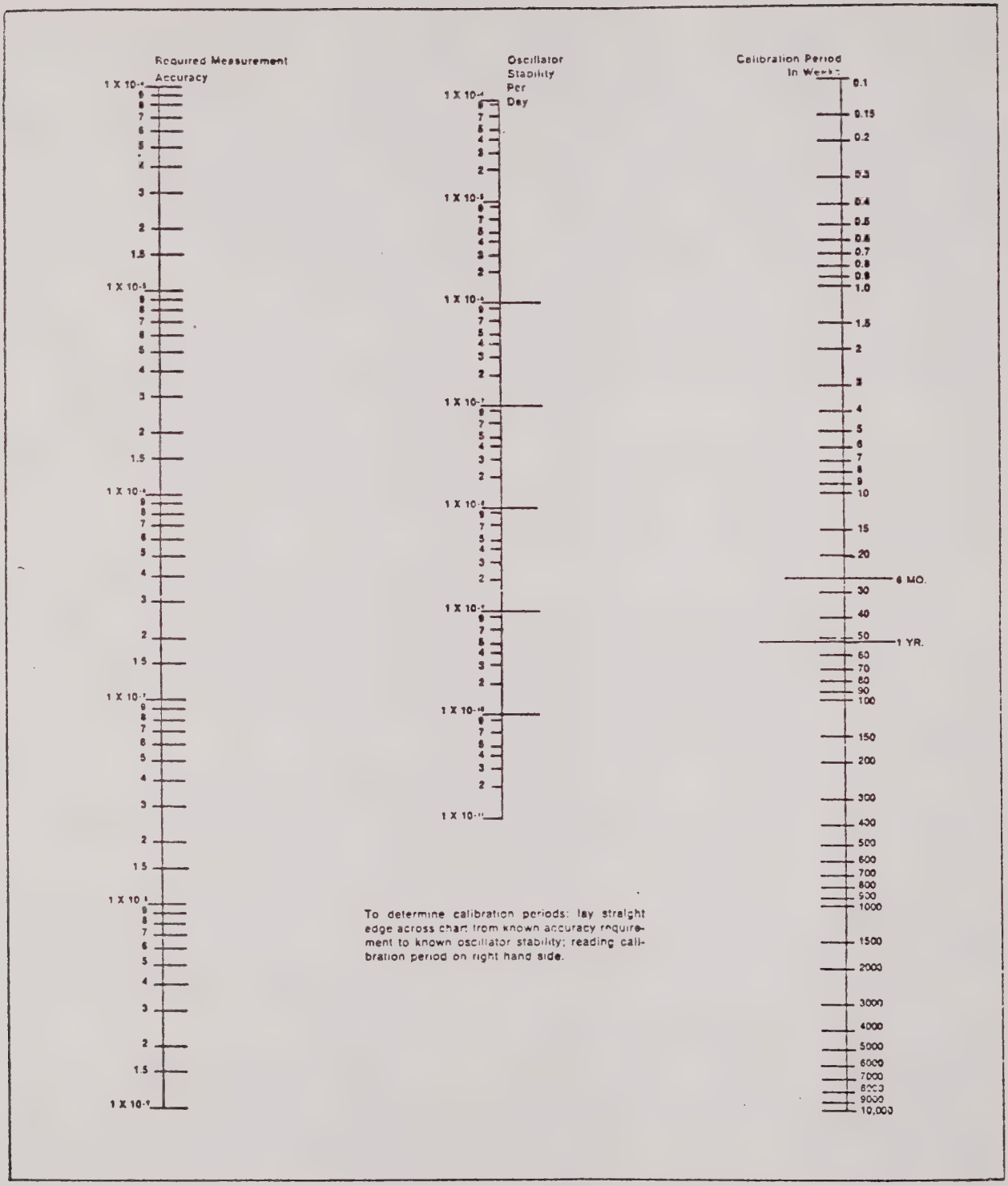

Required Measurement Accuracy
Oscillator Stability Per Day
Calibration Period In Weeks
6 MO.
1 YR.
To determine calibration periods: lay straight edge across chart from known accuracy requirement to known oscillator stability; reading calibration period on right hand side.

FIGURE 5-1 REFERENCE OSCILLATOR CALIBRATION PERIODS

5.4 CHECKOUT PROCEDURE AND INITIAL CONFIDENCE TEST

The following test procedure performs an operational check on the counter and may be used as a confidence check for maintenance purposes, incoming inspection, troubleshooting, etc. The Model 6361A dual counter is described in the following procedure, similar checks on the 6341A and 6351A are identical for the functions that they provide thus this procedure relates to all three counters of the 63X1A series.

1. Insure that the Power Transformer T1 primary is wired for 115V ac operation and that a 1A SLO-BLO fuse is installed in the rear panel fuse holder XF1.

2. Insure that the ac N and H inputs are isolated from the chassis (resistance check).

3. Insure that the ac ground input is connected to the chassis (resistance check).

4. Insure that the +15V, -5.2V, +18V and -18V buses are not grounded or connected together (resistance check).

5. Apply 115V ac power to the rear panel 115V connector and place the front panel POWER toggle switch to it's on (up) position.

6. Measure and verify the following rear panel voltage regulator outputs.

U101	-5.2V	± .25V
U102	+5V	± .25V

7. Measure and verify the following 100 MHz Amplifier (A2 and/or A4) voltage regulator outputs.

U4	-15V	± .25V
U5	+15V	± .25V

8. Using TEE, 50Ω terminators and coax cables connect the rear panel 10 MHz OUTPUT BCN connector to the front panel A and B INPUT BNC connectors and terminate both inputs at 50Ω.

9. Set the front panel signal conditioning controls as follows:

TRIGGER LEVEL to PRESET
ATTENUATOR to X1 AC/DC to AC.

10. Set the front panel RUN/HOLD switch to RUN and observe the display as indicated in Table 5-2 for the appropriate Function, Resolution and Slope settings. All display reading are ±1 count.

5.5 100 MHz AMPLIFIER ASSEMBLY A2 AND A4 PERFORMANCE TEST AND ADJUSTMENT PROCEDURE

Figure 5-2 provides the location of the adjustments and test points required to perform the following procedure. These adjustment and test points are located on the component side of the A2 and A4 PCB's, and can be accessed from the top of the counter.

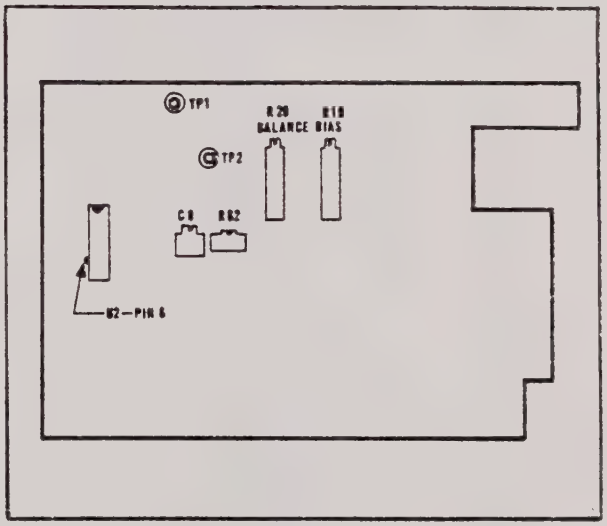


FIGURE 5-2
A2 AND A4 TEST AND ADJUSTMENT LOCATION DIAGRAM

5.5.1 Input Sensitivity Performance Test

1. Select the X1 ATTENUATOR function by pressing the X1 Selector switch.

2. Rotate the TRIGGER LEVEL control fully counter clockwise to it's PRESET position.

TABLE 5-2 DISPLAY READOUT CHECK

Channel	Function	Slope	Resolution	Gate	O.S.	Display	Legend
A and B	Rate	N/A	100 Hz	Blinks	Off	10000.0	kHz
A and B	Rate	N/A	10 Hz	Blinks	Off	10000.00	kHz
A and B	Rate	N/A	1 Hz	Blinks	Off	10000.000	kHz
A and B	Rate	N/A	.1 Hz	Blinks	On	0000.0000	kHz
A and B	Period	N/A	10 ns	Blinks	Off	0.10	μs
A and B	Period	N/A	100 ns	Blinks	Off	0.1	μs
A and B	Period	N/A	1 μs	Blinks	Off	0.	μs
A and B	Period	N/A	10 μs	Blinks	Off	0.00	ms
A and B	TIM	A- B-	10 ns	Blinks	Off	0.10	μs
A and B	TIM	A+ B-	10 ns	Blinks	Off	0.04	μs
A and B	TIM	A- B+	10 ns	Blinks	Off	0.06	μs
A and B	TIM	A- B-	100 ns	Blinks	Off	0.1	μs
A and B	TIM	A+ B+	100 ns	Blinks	Off	0.1	μs
A and B	TIM	A+ B+	1 μs	Blinks	Off	0.	μs
A and B	TIM	A+ B+	10 μs	Blinks	Off	0.00	ms
B	Ratio B/A	N/A	N/A	Blinks	Off	1.	none
A	Alternate	N/A	10 ns	On	Off	0.10	μs
A	Alternate	N/A	100 ns	On	Off	0.1	μs
A	Alternate	N/A	1 μs	On	Off	0.	μs
A	Alternate	N/A	10 μs	On	Off	0.00	ms

NOTE: Alternate Period overrides the B Channel function.

3. Terminate the appropriate INPUT BNC connector at 50Ω.

4. Select the RATE function by pressing the appropriate RATE function switch.

5. Apply 1 MHz at a level of 10 mV (-27 dBm) and verify that the counter reads 1 MHz.

6. Increase the frequency of the applied signal to 10 MHz and verify that the counter reads 10 MHz.

7. Increase the frequency of the applied signal in 10 MHz increments and verify proper counter readings to 100 MHz.

8. Increase the level of the applied signal to 250 mV (+1 dBm) and repeat the verification of the counter's readout in 10 MHz increments from 1 MHz to 100 MHz.

5.5.2 100 MHz Amplifier Alignment Procedure

1. Select the X1 ATTENUATOR function by pressing the X1 selector switch.

2. Rotate the TRIGGER LEVEL control fully counter clockwise to it's PRESET position.

3. Adjust potentiometer R19 (BIAS) for a -1.30V dc reading at test point TP1.

4. Adjust potentiometer R20 (BALANCE) for a -1.30V dc reading at test point TP2.

5. Select the RATE function by pressing the appropriate RATE function switch.

6. Select 100 Hz FREQUENCY RESOLUTION by pressing the 100 Hz switch.

7. Configure a Sweep Generator for a 10 kHz -33 dBm output signal and apply it to the appropriate INPUT BNC connector.

8. Rotate potentiometer R62 fully counter clockwise, then slowly rotate it clockwise to a point that just allows the counter to count and display 10 kHz.

9. Repeat steps 3 and 4 with the 10 kHz -33 dBm signal applied, then repeat step 8.

10. Configure the Sweep Generator for a 0 to 200 MHz sweep output at a -30 dBm output level.

11. Monitor the signal at U2 pin 6 with an Oscilloscope and adjust trimmer capacitor C8 for a "clean" waveform (no dropouts and a flat response of the swept 0 to 200 MHz signal).

5.5 INTEGRATED CIRCUITS COMPONENTS DATA

The major IC components in the 63X1A Counter Timers are described in this section to aid in circuit description, troubleshooting and repair of the unit. Components are not described in complete detail but are extracts from the manufacturer's specification catalog. For those IC's not described or if more significant characteristics are required, refer to the appropriate manufacturer's specification sheet and/or catalog. Table 5-3 lists the IC's in alphanumeric manufacturer's part number order.

TABLE 5-3 I.C. COMPONENT DESCRIPTIONS

COMPONENT NUMBER	TITLE	S-D PART NUMBER	PAGE
CA3018	Linear 4 Transistor Array	025720	5-6
CA3130T	Linear Operational Amplifier	103231	5-7
MC1648	ECL Voltage Controlled Oscillator (VCO)	045236	5-10
MC78L15ACP	+15V Low Power Voltage Regulator	117260	5-11
MC79L15ACP	−15V Low Power Voltage Regulator	117261	5-12
MC10100P	ECL Quad 2-Input NOR Gate With Strobe	103712	5-13
MC10101P	ECL Quad OR/NOR Gate	025791	5-13
MC10102P	ECL Quad 2-Input NOR Gate	103025	5-14
MC10124P	ECL Quad TTL-To-ECL Translator	045228	5-15
MC10125P	ECL Quad ECL-To-TTL Translator	106660	5-16
MC10129P	ECL Quad Bus Receiver		5-17
MC10138P	ECL Quad Bi-Quinary Counter	103837	5-18
MC10216L	ECL High Speed Triple Line Receiver	045276	5-19
MC10231P	ECL Dual Type D M-S Flip-Flop	045227	5-20
MC12040P	ECL Phase-Frequency Detector	045277	5-22
MC14050	CMOS Hex Inverter Buffer	103492	5-23
NE555V	Monolithic Timer	045208	5-24
SD055095	CMOS LSI Counter System, IC Data Sheet	055095	5-25
SD057306	TTL ROM Programmed 63X1A M.U. And D.P.	057306	5-27
SN74LS00N	TTL Low Power Schottky Quad 2-Input NAND Gate	103130	5-28
SN74LS04N	Hex Inverter	103749	5-29
SN74LS08N	TTL Low Power Schottky Quad 2-Input AND Gate	103967	5-30
SN74LS10N	Triple 3-Input Positive-NAND Gate	103968	5-31
SN7416N	Hex Inverter Buffer/Driver With Open-Collector High Voltage Outputs	045230	5-32
SN7417N	TTL Hex Buffer/Driver	106629	5-32
SN74LS30N	TTL Low Power Schottky 8-Input NAND Gate	103971	5-33
SN74LS32N	TTL Quad 2-Input OR Gate	103972	5-33
SN7490N	MSI TTL High-Speed Decade Counter	025732	5-34
SN74LS123N	TTL Low Power Schottky Retriggerable One-Shot M.V.	103976	5-35
SN74LS196N	TTL Low Power Schottky 30 MHz Presettable	103164	5-36
SN74247N	TTL BCD-To-Seven Segment Decoder/Driver	103314	5-37

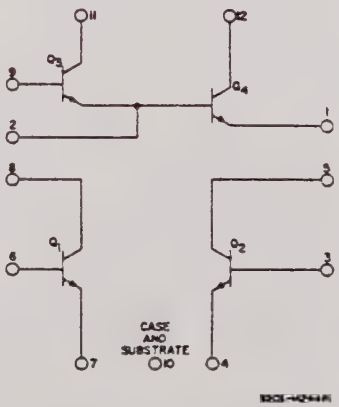
The CA3018 and CA3018A consist of four general purpose silicon n-p-n transistors on a common monolithic substrate.

Two of the four transistors are connected in the Darlington configuration. The substrate is connected to a separate terminal for maximum flexibility.

The transistors of the CA3018 and the CA3018A are well suited to a wide variety of applications in low-power systems in the DC through VHF range. They may be used as discrete transistors in conventional circuits but in addition they provide the advantages of close electrical and thermal matching inherent in integrated circuit construction.

The CA3018A is similar to the CA3018 but features tighter control of current gain, leakage, and offset parameters making it suitable for more critical applications requiring premium performance.

12-Lead
TO-5 Style



Schematic Diagram for CA3018 and CA3018A

CA3130T

S-D P/N 103231

8-LEAD TO-5 with Dual-In-Line Formed Leads (S suffix)

H-1787

8-LEAD TO-5 (T suffix)

H-1528

COS/MOS Operational Amplifiers

With MOS/FET Input

Features:

- MOS/FET input stage provides:
  - very high Z_I = 1.5 TΩ (1.5 x 10^{12} Ω) typ.
  - very low I_I = 5 pA typ. at 15 V operation
  - 2 pA typ. at 5 V operation
- Common-mode input-voltage range includes negative supply rail; input terminals can be swung 0.5 V below negative supply rail
- COS/MOS output stage permits signal swing to either (or both) supply rails

} Ideal for single-supply applications

- Low V_{IO}: 2 mV max. (CA3130B)
- Wide BW: 15 MHz typ. (unity-gain crossover)
- High SR: 10 V/μs typ. (unity-gain follower)
- High output current (I_O): 20 mA typ.
- High A_{OL}: 320,000 (110 dB) typ.
- Compensation with single external capacitor

Applications:

- Ground-referenced single-supply amplifiers
- Fast sample-hold amplifiers
- Long-duration timers/monostables
- High-input-impedance comparators (ideal interface with digital COS/MOS)
- High-input-impedance wideband amplifiers
- Voltage followers (e.g., follower for single-supply D/A converter)
- Voltage regulators (permits control of output voltage down to zero volts)
- Peak detectors
- Single-supply full-wave precision rectifiers
- Photo-diode sensor amplifiers

RCA-CA3130T, CA3130S, CA3130AT, CA3130AS, CA-3130BT, and CA3130BS are integrated-circuit operational amplifiers that combine the advantages of both COS/MOS and bipolar transistors on a monolithic chip.

Gate-protected p-channel MOS/FET (PMOS) transistors are used in the input circuit to provide very-high-input impedance, very-low-input current, and exceptional speed performance. The use of PMOS field-effect transistors in the input stage results in common-mode input-voltage capability down to 0.5 volt below the negative-supply terminal, an important attribute in single-supply applications.

A complementary-symmetry MOS (COS/MOS) transistor pair, capable of swinging the output voltage to within millivolts of either supply-voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA3130 Series circuits operate at supply voltages ranging from 5 to 16 volts, or ±2.5 to ±8 volts when using split supplies. They can be phase compensated with a single external capacitor, and have terminals for adjustment of offset voltage for applications requiring offset-null capability. Terminal provisions are also made to permit strobing of the output stage.

The CA3130 Series is supplied in either the standard 8-lead TO-5-style package (T suffix) or in the 8-lead dual-in-line formed-lead TO-5-style package "DIL-CAN" (S suffix) and operates over the full military-temperature range of −55°C to +125°C. The CA3130B is intended for applications requiring premium-grade specifications and with limits established for: input current, temperature coefficient of input-offset voltage, and gain over the range of −55°C to +125°C. The CA3130A offers superior input characteristics over those of the CA3130.

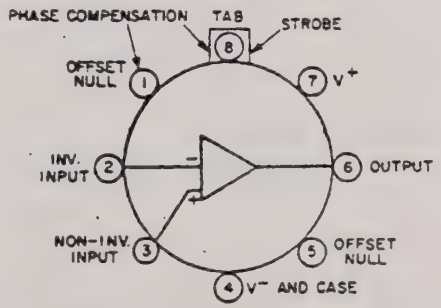
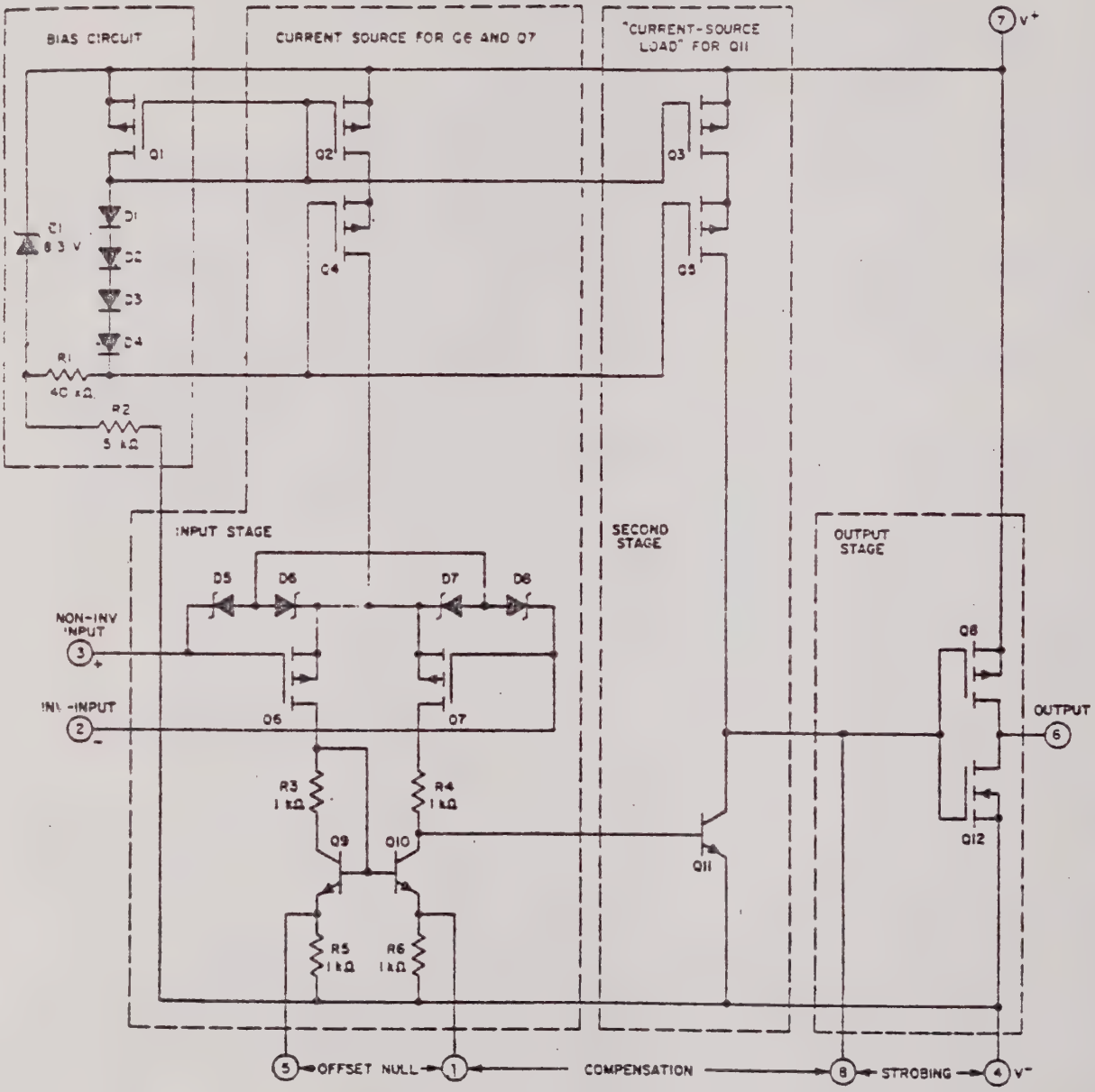


Fig. 1—Functional diagram of the CA3130 Series.

CA3130T

S-D P/N 103231



NOTE:
DIODES D5 THROUGH D8 PROVIDE GATE-OXIDE PROTECTION FOR MOS/FET INPUT STAGE.

Fig. 2—Schematic diagram of the CA3130 Series.

CA3130T

S-D P/N 103231

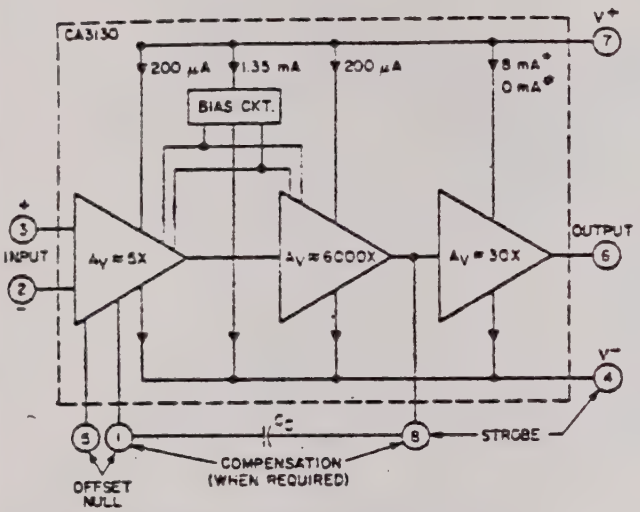


Fig. 3—Block diagram of the CA3130 Series.

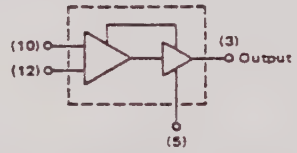
transistors Q2, Q4 are the constant-current source for the input stage. The biasing circuit for the constant-current source is subsequently described. The small diodes D5 through D8 provide gate-oxide protection against high-voltage transients, e.g. including static electricity during handling for Q6 and Q7.

Second Stage—Most of the voltage gain in the CA3130 is provided by the second amplifier stage, consisting of bipolar transistor Q11 and its cascode-connected load resistance provided by PMOS transistors Q3 and Q5. The source of bias potentials for these PMOS transistors is subsequently described. Miller-Effect compensation (roll-off) is accomplished by simply connecting a small capacitor between Terms. 1 and 8. A 47-picofarad capacitor provides sufficient compensation for stable unity-gain operation in most applications.

Bias-Source Circuit—At total supply voltages, somewhat above 8.3 volts, resistor R2 and zener diode Z1 serve to establish a voltage of 8.3 volts across the series-connected circuit, consisting of resistor R1, diodes D1 through D4, and PMOS transistor Q1. A tap at the junction of resistor R1 and diode D4 provides a gate-bias potential of about 4.5 volts for PMOS transistors Q4 and Q5 with respect to Term. 7. A potential of about 2.2 volts is developed across diode-connected PMOS transistor Q1 with respect to Term. 7 to provide gate bias for PMOS transistors Q2 and Q3. It should be noted that Q1 is "mirror-connected"† to both Q2 and Q3. Since transistors Q1, Q2, Q3 are designed to be identical, the approximately 200-microampere current in Q1 establishes a similar current in Q2 and Q3 as constant-current sources for both the first and second amplifier stages, respectively.

At total supply voltages somewhat less than 8.3 volts, zener diode Z1 becomes non-conductive and the potential, developed across series-connected R1, D1-D4, and Q1, varies directly with variations in supply voltage. Consequently, the gate bias for Q4, Q5 and Q2, Q3 varies in accordance with supply-voltage variations. This variation results in deterioration of the power-supply-rejection ratio (PSRR) at total supply voltages below 8.3 volts. Operation at total supply voltages below about 4.5 volts results in seriously degraded performance.

Output Stage—The output stage consists of a drain-loaded inverting amplifier using COS/MOS transistors operating in the Class A mode. When operating into very high resistance loads, the output can be swung within millivolts of either supply rail. Because the output stage is a drain-loaded amplifier, its gain is dependent upon the load impedance. The transfer characteristics of the output stage for a load returned to the negative supply rail are shown in Fig. 6. Typical op-amp loads are readily driven by the output stage. Because large-signal excursions are non-linear, requiring feedback for good waveform reproduction, transient delays may be encountered. As a voltage follower, the amplifier can achieve 0.01 per cent accuracy levels, including the negative supply rail.



Numbers in parenthesis denote pin number for F package (Case 607) L package (Case 632), and P package (Case 646).

Input Capacitance = 6 pF typ
Maximum Series Resistance for L (External Inductance) = 50 Ω typ
Power Dissipation = 150 mW typ/pkg (+5.0 Vdc Supply)
Maximum Output Frequency = 225 MHz typ

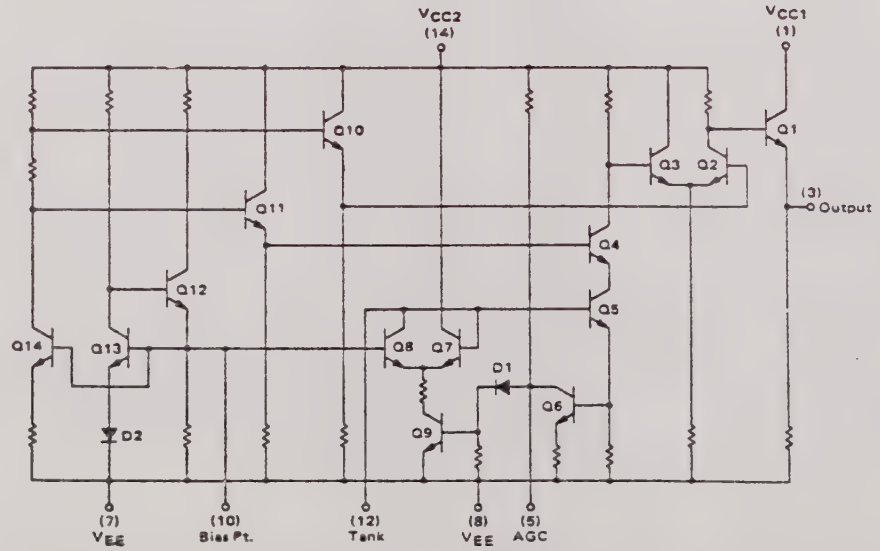
The MC1648 is an emitter-coupled oscillator, constructed on a single monolithic silicon chip. Output levels are compatible with MECL III logic levels. The oscillator requires an external parallel tank circuit consisting of the inductor (L) and capacitor (C).

A varactor diode may be incorporated into the tank circuit to provide a voltage variable input for the oscillator (VCO). The MC1648 was designed for use in the Motorola Phase-Locked Loop shown in Figure 8. This device may also be used in many other applications requiring a fixed or variable frequency clock source of high spectral purity (See Figure 2).

The MC1648 may be operated from a +5.0 Vdc supply or a -5.2 Vdc supply, depending upon system requirements.

SUPPLY VOLTAGE	GND PINS	SUPPLY PINS
+5.0 Vdc	7, 8	1, 14
-5.2 Vdc	1, 14	7, 8

FIGURE 1 – CIRCUIT SCHEMATIC



Numbers in parenthesis denote pin number for F package (Case 607), L package (Case 632), and P package (Case 646).

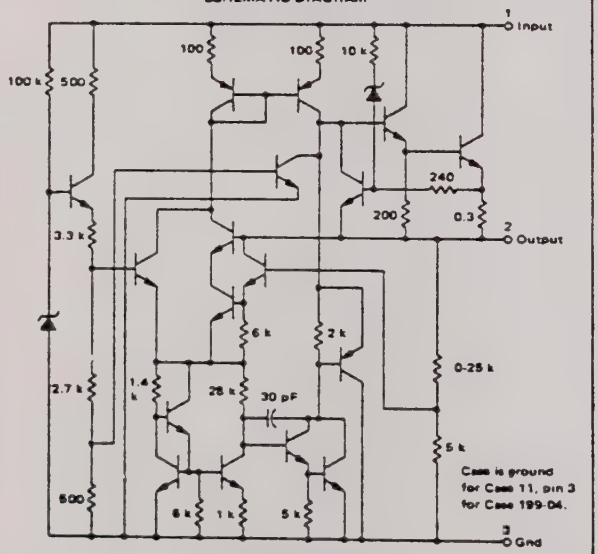
MC78L15ACP S-D P/N 117260

MC7800C SERIES THREE-TERMINAL POSITIVE VOLTAGE REGULATORS

The MC7800C Series of three-terminal positive voltage regulators are monolithic integrated circuits designed as fixed-voltage regulators for a wide variety of applications including local, on-card regulation. Available in seven fixed output voltage options from 5.0-to-24 volts, these regulators employ internal current limiting, thermal shutdown, and safe area compensation – making them essentially blow-out proof. With adequate heatsinking they can deliver output currents in excess of 1.0 ampere. The last two digits of the part number indicate nominal output voltage.

- Output Current in Excess of 1.0 Ampere
- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Packaged in the Plastic Case 199-04
  (Pin Compatible with the VERSAWATT† or TO-220)
  Or Hermetic TO-3 Type Metal Power Package (Case 11)

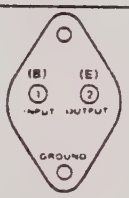
SCHEMATIC DIAGRAM



TYPE NO./VOLTAGE

MC7805C 5.0 Volts	MC7808C 8.0 Volts	MC7818C 18 Volts
MC7806C 6.0 Volts	MC7812C 12 Volts	MC7824C 24 Volts
	MC7815C 15 Volts	

K SUFFIX
METAL PACKAGE
CASE 11
(TO-3 TYPE)



(bottom view)

Pins 1 and 2 electrically isolated from case.
Case is third electrical connection.

P SUFFIX
PLASTIC PACKAGE
CASE 199-04

Pin 1 Input (Base)
Pin 2 Output (Emitter)
Pin 3 Ground (Collector)

Heat sink surface connected to pin 3.

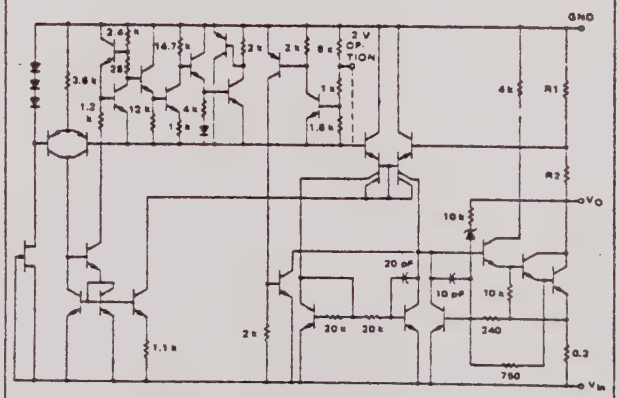
MC7900C SERIES THREE-TERMINAL NEGATIVE VOLTAGE REGULATORS

The MC7900C Series of fixed output negative voltage regulators are intended as complements to the popular MC7800C Series devices. These negative regulators are available in the same seven-voltage options as the MC7800C devices. In addition, two extra voltage options commonly employed in MECL systems are also available in the negative MC7900C Series.

Available in fixed output voltage options from -2.0 to -24 volts, these regulators employ current limiting, thermal shutdown, and safe-area compensation — making them remarkably rugged under most operating conditions. With adequate heat-sinking they can deliver output currents in excess of 1.0 ampere.

- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Packaged in the Plastic Case 199-04
  (Pin Compatible with the VERSAWATT† or TO-220)
  Or Hermetic TO-3 Type Metal Power Package

SCHEMATIC DIAGRAM



DEVICE TYPE/NOMINAL OUTPUT VOLTAGE

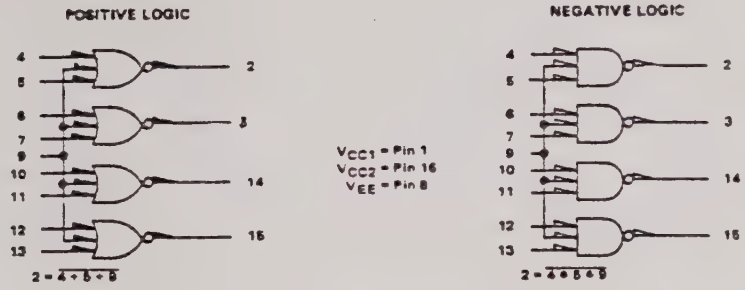
MC7902C - 2.0 Volts	MC7906C - 6.0 Volts	MC7915C - 15 Volts
MC7905C - 5.0 Volts	MC7908C - 8.0 Volts	MC7918C - 18 Volts
MC7905.2C - 5.2 Volts	MC7912C - 12 Volts	MC7924C - 24 Volts

ECL QUAD 2-INPUT NOR GATE WITH STROBE

MC10100 S-D P/N 103712

The MC10100 is a quad NOR gate. Each gate has 3 inputs, two of which are independent and one of which is tied common to all four gates. Input pulldown resistors eliminate the need to tie unused inputs to a voltage supply. Open emitter outputs permit wire-ORing and direct connection to busses.

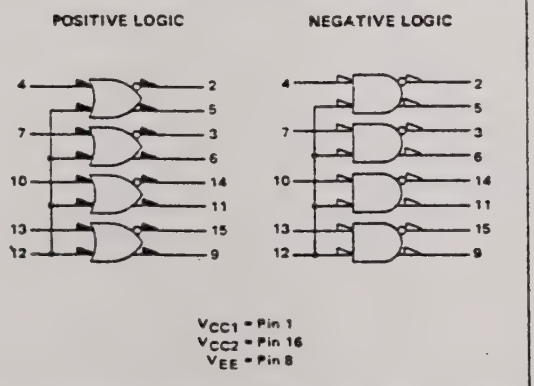
P_D = 25 mW typ/gate (No Load)
t_{pd} = 2.0 ns typ



ECL QUAD OR/NOR GATE

MC10101 S-D P/N 025791

The MC10101 is a quad 2-input OR/NOR gate with one input from each gate common to pin 12. Input pulldown resistors eliminate the need to tie unused inputs to an external supply.

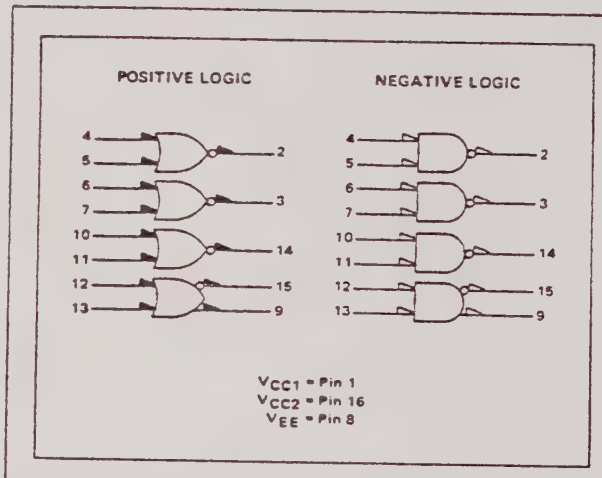


P_D = 25 mW typ/gate (No Load)
t_{pd} = 2.0 ns typ
Output Rise and Fall Time:
= 3.5 ns typ (10% - 90%)
= 2.0 ns typ (20% - 80%)

ECL QUAD 2-INPUT NOR GATE

MC10102

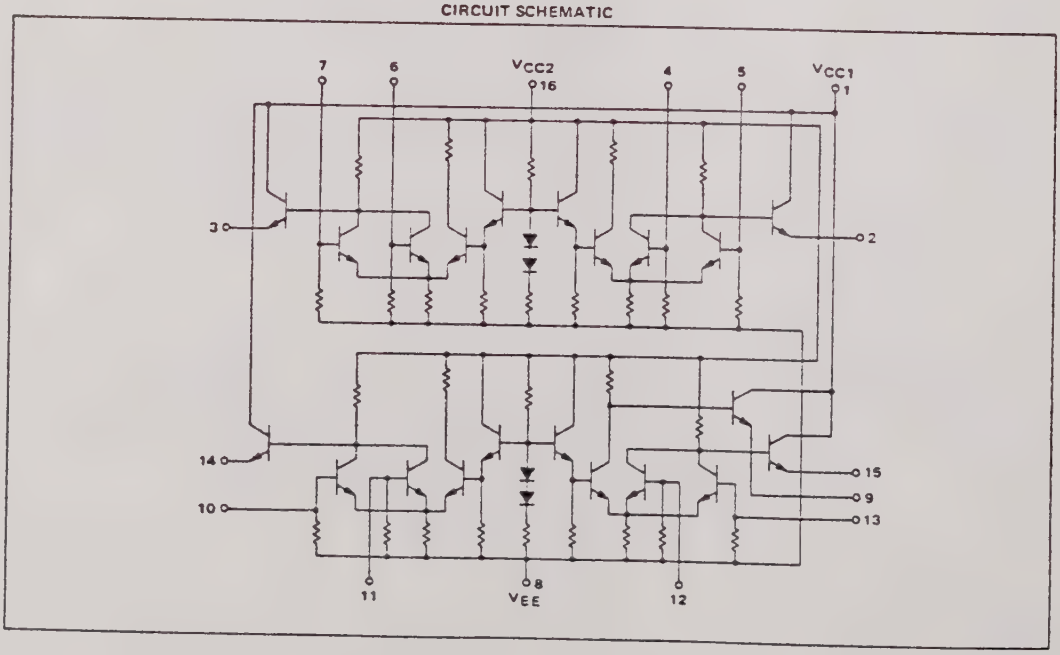
S-D P/N 103025



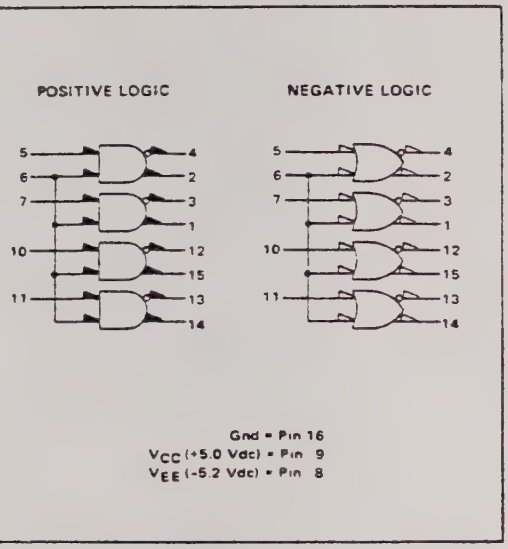
The MC10102 is a quad 2-input NOR gate. Input pulldown resistors eliminate the need to tie unused inputs to an external supply.

P_D = 25 mW typ/gate (No Load)
t_{pd} = 2.0 ns typ
Output Rise and Fall Time:
= 3.5 ns typ (10% - 90%)
= 2.0 ns typ (20% - 80%)

CIRCUIT SCHEMATIC



63X1A-178



The MC10124 is a quad translator for interfacing data and control signals between a saturated logic section and the MECL section of digital systems. The MC10124 has MTTL compatible inputs, and MECL complementary open-emitter outputs that allow use as an inverting/non-inverting translator or as a differential line driver. When the common strobe input is at the low logic level, it forces all true outputs to a MECL low logic state and all inverting outputs to a MECL high logic state.

Power supply requirements are ground, +5.0 Volts, and -5.2 Volts. Propagation delay of the MC10124 is typically 5.0 ns. The dc levels are standard or Schottky MTTL in, MECL 10,000 out.

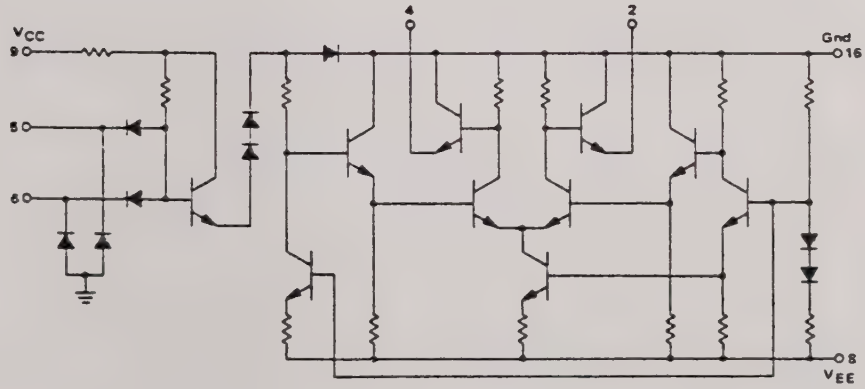
An advantage of this device is that MTTL level information can be transmitted differentially, via balanced twisted pair lines, to the MECL equipment, where the signal can be received by the MC10115 or MC10116 differential line receivers. The MC10124 is useful in computers, instrumentation, peripheral controllers, test equipment, and digital communications systems.

P_D = 340 mW typ/pkg (No Load)

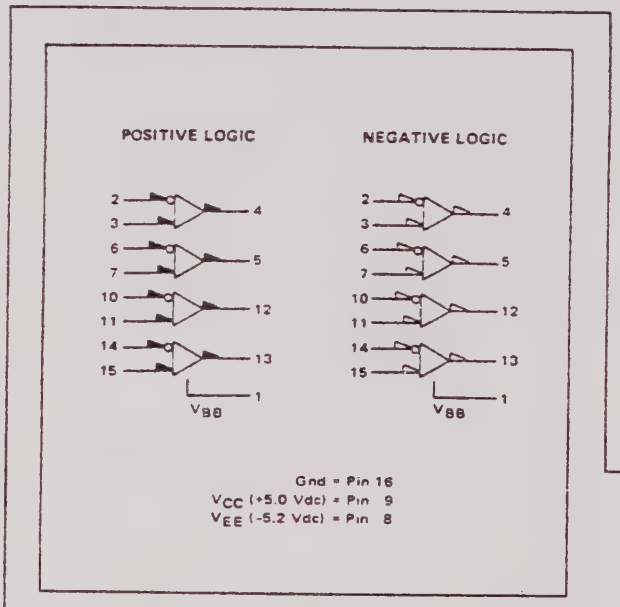
t_{pd} = 5.0 ns typ (+ 1.5 Vdc in to 50% out)

Output Rise, Fall Times,
2.5 ns typ (20% to 80%)

CIRCUIT SCHEMATIC
1/4 OF CIRCUIT SHOWN



ECL QUAD ECL-TO-TTL TRANSLATOR



The MC10125 is a quad translator for interfacing data and control signals between the MECL section and saturated logic sections of digital systems. The MC10125 incorporates differential inputs and Schottky MTTL "totem pole" outputs. Differential inputs allow for use as an inverting/non-inverting translator or as a differential line receiver. The V_{BB} reference voltage is available on pin 1 for use in Schmitt trigger applications and single-ended input biasing. The outputs of the MC10125 go to a low logic level whenever the inputs are left floating.

Power supply requirements are ground, +5.0 Volts and -5.2 Volts. Propagation delay of the MC10125 is typically 5.0 ns. The MC10125 has fanout of 10 MTTL loads. The dc levels are MECL 10,000 in and Schottky TTL, or MTTL out. This device has an input common mode noise rejection of ±1.0 Volt.

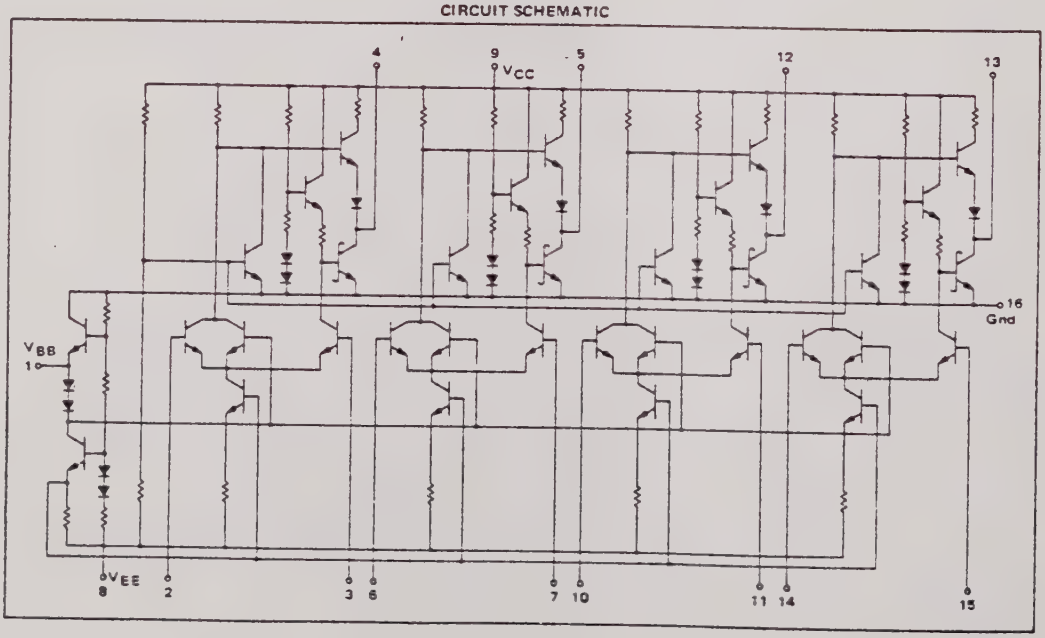
An advantage of this device is that MECL level information can be received, via balanced twisted pair lines, in the MTTL equipment. This isolates the MECL logic from the noisy MTTL environment. This device is useful in computers, instrumentation, peripheral controllers, test equipment and digital communications systems.

P_D = 380 mW typ/pkg (No Load)

t_{pd} = 4.5 ns typ (50% to +1.5 Vdc out)

Output Rise, Fall Times,
2.5 ns typ (20% to 80%)

CIRCUIT SCHEMATIC

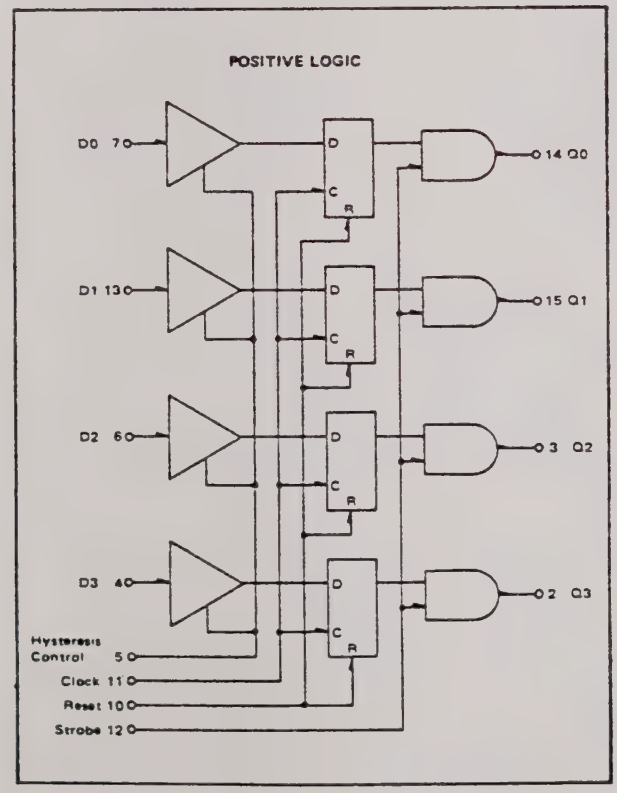


The MC10129 bus receiver works in conjunction with the MC10128 to allow interfacing of MECL 10,000 to other forms of logic and logic buses. The data inputs are compatible with, and accept MTTL logic levels as well as levels compatible with IBM-type buses. The clock, strobe, and reset inputs accept MECL 10,000 logic levels.

The data inputs accept the bus levels, and storage elements are provided to yield temporary latch storage of the information after receiving it from the bus. The outputs can be strobed to allow accurate synchronization of signals and/or connection to MECL 10,000 level buses. When the clock is low, the outputs will follow the D inputs, and the reset input is disabled. The latches will store the data on the rising edge of the clock. The outputs are enabled when the strobe input is high. Unused D inputs must be tied to V_{CC} or Gnd. The clock, strobe, and reset inputs each have 50 k ohm pulldown resistors to V_{EE}. They may be left floating, if not used.

The MC10129 will operate in either of two modes. The first mode is obtained by tying the hysteresis control input to V_{EE}. In this mode, the input threshold points of the D inputs are fixed. The second mode is obtained by tying the hysteresis control input to ground. In this mode, input hysteresis is achieved as shown in the test table. This hysteresis is desirable where extra noise margin is required on the D inputs. The other input pins are unaffected by the mode of operation used.

The MC10129 is especially useful in interface applications for central processors, mini-computers, and peripheral equipment.



TRUTH TABLE

D	C	STROBE	RESET	Q_{n+1}
Φ	Φ	L	Φ	L
Φ	H	Φ	H	L
L	L	H	Φ	L
Φ	H	H	L	Q_n
H	L	H	Φ	H

Φ = Don't Care

P_D = 750 mW typ/pkg (No Load)
t_{pd} = 10 ns typ

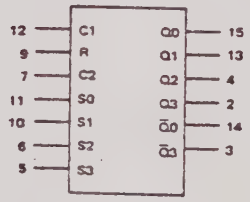
V_{CC} = Pin 9
Gnd = Pins 1 and 16
V_{EE} = Pin 8

The MC10138 is a four bit counter capable of divide by two, five, or ten functions. It is composed of four set-reset master-slave flip-flops. Clock inputs trigger on the positive going edge of the clock pulse.

Set or reset input override the clock, allowing asynchronous "set" or "clear". Individual set and common reset inputs are provided, as well as complementary outputs for the first and fourth bits. True outputs are available at all bits.

P_D = 370 mW typ/pkg (No Load)
f_{tog} = 150 MHz typ

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8



COUNTER TRUTH TABLES

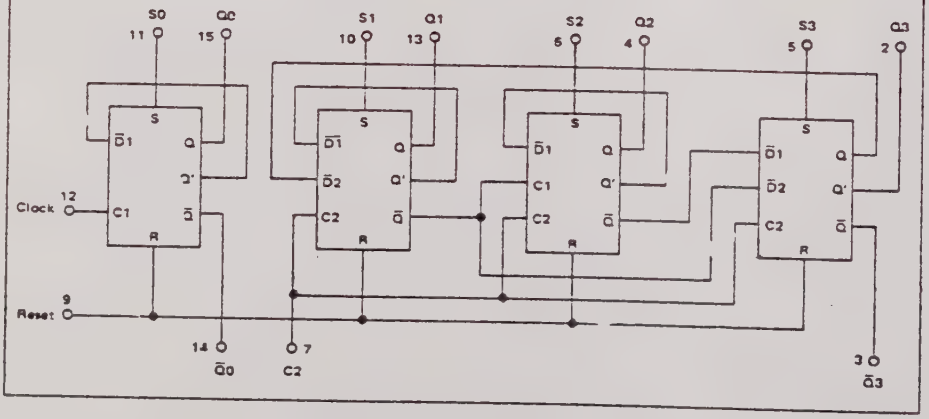
BI-QUINARY
(Clock connected to C2 and Q3 connected to C1)

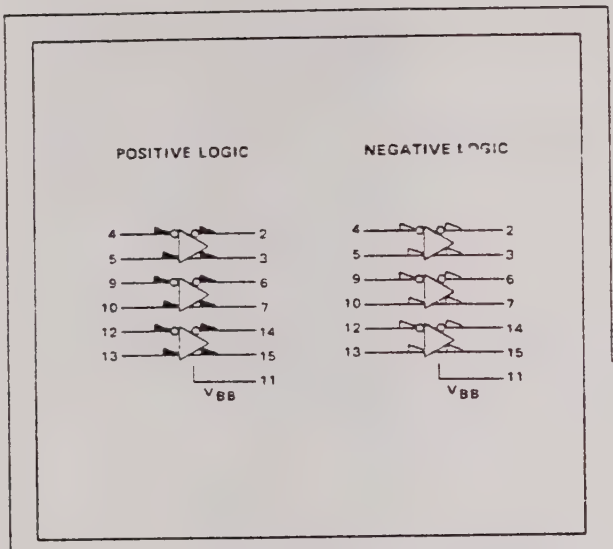
COUNT	Q1	Q2	Q3	Q0
0	L	L	L	L
1	L	L	L	H
2	L	H	L	L
3	L	H	L	H
4	L	L	H	L
5	L	L	H	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BCD
(Clock connected to C1 and Q0 connected to C2)

COUNT	Q0	Q1	Q2	Q3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

BLOCK DIAGRAM





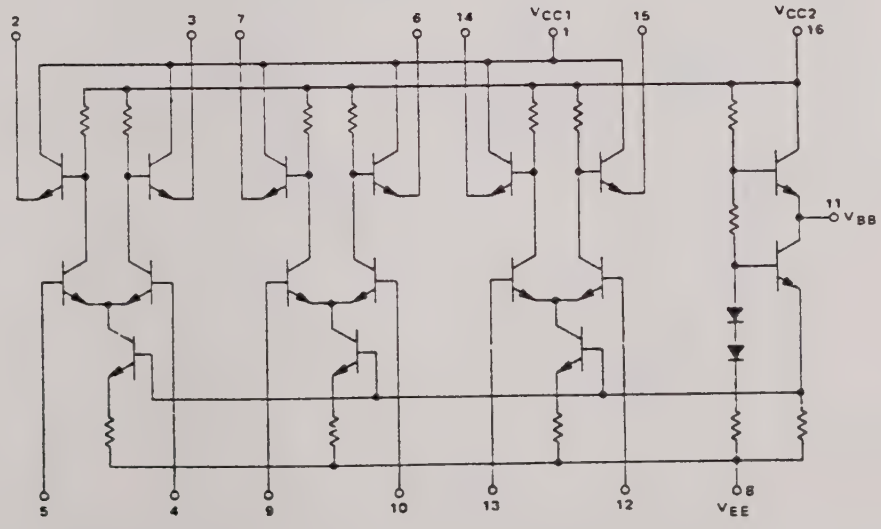
The MC10216 is a high speed triple differential amplifier designed for use in sensing differential signals over long lines. The base bias supply (V_{BB}) is made available at pin 11 to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

Active current sources provide the MC10216 with excellent common mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} (pin 11) to prevent upsetting the current source bias network.

Complementary outputs are provided to allow driving twisted pair lines, to enable cascading of several amplifiers in a chain, or simply to provide complement outputs of the input logic function.

P_D = 90 mW typ/pkg

CIRCUIT SCHEMATIC



R-S TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

N.D. = Not Defined

CLOCKED TRUTH TABLE

C	D	Q_{n+1}
L	φ	Q_n
H	L	L
H	H	H

φ = Don't Care

$C = \overline{C}_E \cdot C_C$

A clock H is a clock transition from a low to a high state.

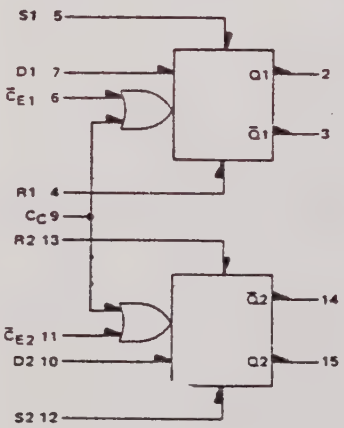
The MC10231 is a dual master-slave type D flip-flop. Asynchronous set (S) and reset (R) override clock (C_C) and clock enable (C_E) inputs. Each flip-flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip-flop, the clock enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data (D) input will not affect the output information at any other time due to master slave construction.

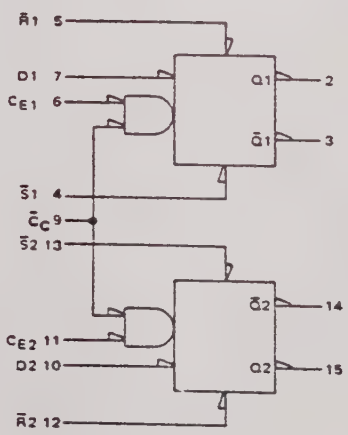
Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}. Output rise and fall times allow high frequency operation over 200 MHz.

P_D = 225 mW typ/pkg (No Load)
f_{Tog} = 225 MHz typ

POSITIVE LOGIC



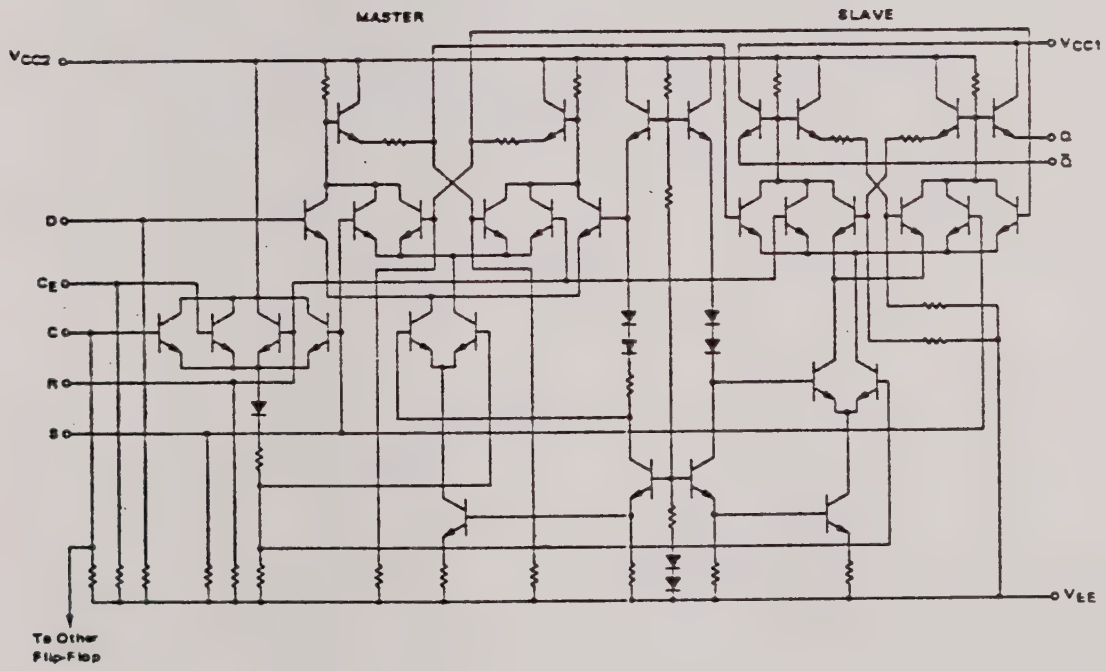
NEGATIVE LOGIC

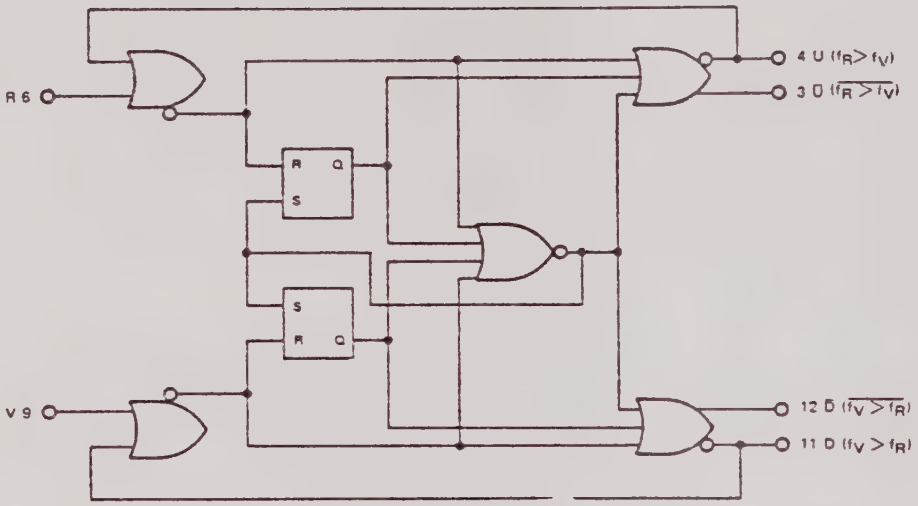


V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

MC10231 S-D P/N 045227

CIRCUIT SCHEMATIC
1/2 OF CIRCUIT SHOWN





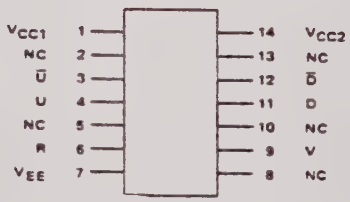
V_{CC1} = Pin 1
V_{CC2} = Pin 14
V_{CC3} = Pin 7

The MC12040 is a logic network designed for use as a phase comparator for MECL-compatible input signals. It determines the "lead" or "lag" phase relationship and the time difference between the leading edges of the waveforms. Since these edges occur only once per cycle, the detector has a range of $\pm 2\pi$ radians.

Operation of the device may be illustrated by assuming two waveforms, R and V (Figure 1), of the same frequency but differing in phase. If the logic had established by past history that R was leading V, the U output of the detector (pin 4) would produce a positive pulse width equal to the phase difference and the D output (pin 11) would simply remain low.

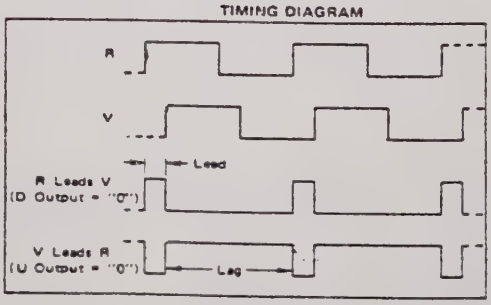
On the other hand, it is also possible that V was leading R (Figure 1), giving rise to a positive pulse on the D output and a constant low level on the U output pin. Both outputs for the sample condition are valid since the determination of lead or lag is dependent on past edge crossing and initial conditions at start-up. A stable phase-locked loop will result from either condition.

Phase error information is contained in the output duty cycle — that is, the ratio of the output pulse width to total period. By integrating or low-pass filtering the outputs of the detector and shifting the level to accommodate ECL swings, usable analog information for the voltage-controlled oscillator can be developed.



NC — No Connection

TIMING DIAGRAM



MC14049
MC14050

S-D P/N 103217
S-D P/N 103492

HEX BUFFERS

The MC14049B hex inverter/buffer and MC14050B noninverting hex buffer are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS devices find primary use where low power dissipation and/or high noise immunity is desired. These devices provide logic-level conversion using only one supply voltage, V_{CC}. The input-signal high level (V_{IH}) can exceed the V_{CC} supply voltage for logic-level conversions. Two TTL/DTL Loads can be driven when the devices are used as CMOS-to-TTL/DTL converters (V_{CC} = 5.0 V, $V_{OL} \leq$ 0.4 V, $I_{OL} \geq$ 3.2 mA). Note that pin 16 is not connected internally on these devices; consequently connections to this terminal will not affect circuit operation.

- High Source and Sink Currents
- High-to-Low Level Converter
- Quiescent Current = 2.0 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc

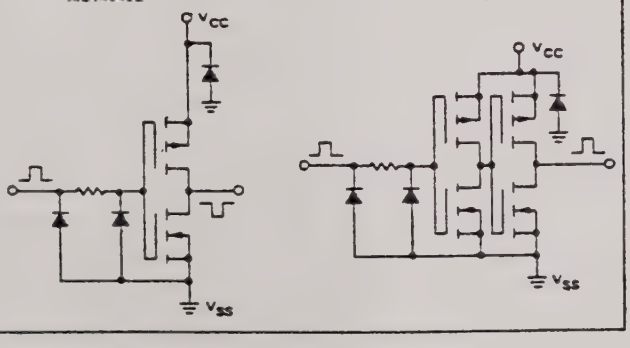
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

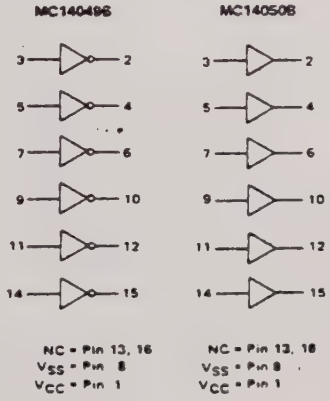
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

CIRCUIT SCHEMATIC
(1/6 OF CIRCUIT SHOWN)



LOGIC DIAGRAMS



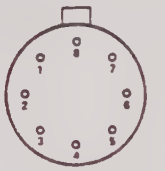
NC = Pin 13, 16
V_{SS} = Pin 8
V_{CC} = Pin 1

NC = Pin 13, 16
V_{SS} = Pin 8
V_{CC} = Pin 1

DESCRIPTION

The NE/SE 555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA or drive TTL circuits.

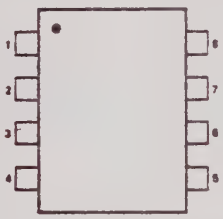
PIN CONFIGURATIONS



T PACKAGE
(Top View)

1. Ground
2. Trigger
3. Output
4. Reset
5. Control Voltage
6. Threshold
7. Discharge
8. V_{CC}

ORDER PART NOS. SE555T/NE555T

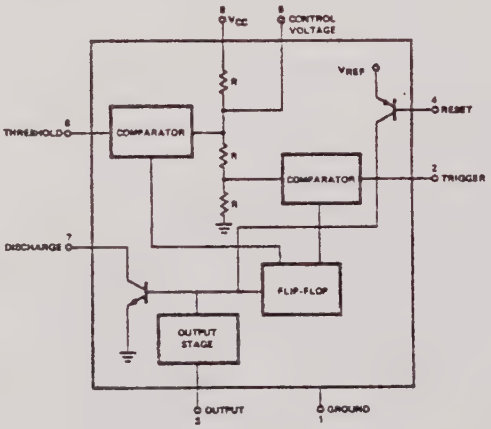


V PACKAGE
(Top View)

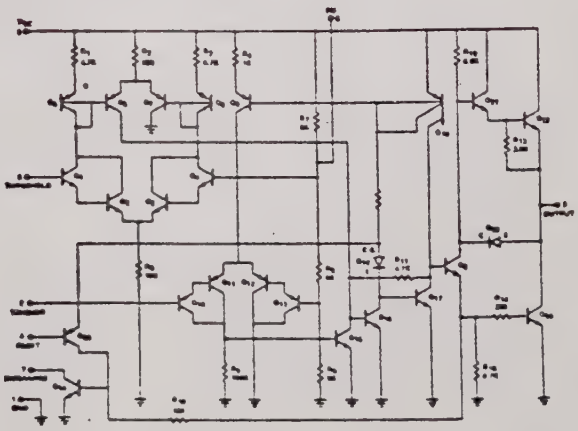
1. Ground
2. Trigger
3. Output
4. Reset
5. Control Voltage
6. Threshold
7. Discharge
8. V_{CC}

ORDER PART NOS. SE555V/NE555V

BLOCK DIAGRAM



EQUIVALENT CIRCUIT



SD055095 S-D P/N 055095

The circuitry of this 40 pin CMOS Decade Count Chain contains: a six decade divider chain, an overflow detector, 33-Bit Storage register, a multiplex, an adjustable multiplex free-running M.V. clock, a blank code generator/decimal point activator, and a clock selector allowing for the provision to break the decade chain into two chains of three decades each.

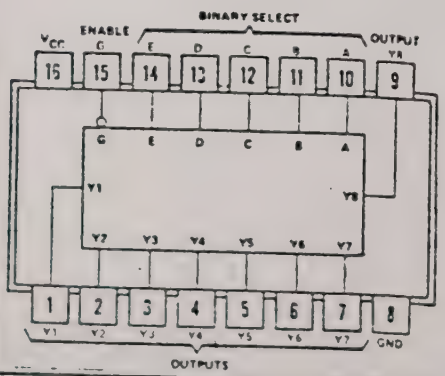
Listed by pin number are the inputs and outputs of the device, with signal name and functional details.

Pin No.	Signal Name	Function
1	TEST CLOCK ENABLE	Allows the three MSD of the decade chain to be driven by the TEST CLOCK when set high.
2	TEST CLOCK	Clock input to the 3rd MSD of the count chain, enabled when the TEST CLOCK ENABLE is set high.
3	LSD 8	LSD Bit "8" input.
4	LSD 4	LSD Bit "4" input.
5	LSD 2	LSD Bit "2" input.
6	LSD 1	LSD Bit "1" input.
7	DECADE CLOCK	Clock input to the LSD decade of the count chain.
8	Not Used	
9	Not Used	
10	SLSD 8	NLSD Bit "8" input.
11	SLSD 4	NLSD Bit "4" input.
12	SLSD 2	NLSD Bit "2" input.
13	SLSD 1	NLSD Bit "1" input.
14	Not Used	
15	Vcc	+ voltage supply input +4.5 to +5.5 Vdc ≤50 mV p-p ripple or noise.
16	BCD1	Multiplexed BCD Bit "1" output.
17	BCD2	Multiplexed BCD Bit "2" output.
18	SUPPLEMENTAL OUTPUT	Carry from the NMSD of the count chain.
19	BCD 4	Multiplexed BCD Bit "4" output.
20	BCD 8	Multiplexed BCD Bit "8" output.
21	BLANK CODE	Indicates that the LSD was present on the BCD output pins. The BLANK CODE will reset (go to logic high) on the detection of the first of the following three conditions; 1) Detection of an Over Flow. 2) Detection of a logic high on any of the BCD outputs. 3) Detection of a coincidence of any of the

Pin No.	Signal Name	Function
21	BLANK CODE (Cont)	position and Octal Code listed as follows: Position — Octal Code 1 — 7 2 — 6 3 — 5 4 — 4 5 — 3 6 — 2 7 — 1 8 — 0
22	DECIMAL POINT	A decimal point actuation when position output coincides with the proper octal code input.
23 24 25	OCTAL CODE BIT 4 OCTAL CODE BIT 2 OCTAL CODE BIT 1	The octal code inputs can be considered as static logic levels, they may be changed at any time, but will not effect outputs until the completion of a full multiplexer cycle.
26	OVER FLOW	Indicates that the MSD of the count chain has generated a carry. This function must be reset by a Master Reset on pin 40, to return to its logic low state.
27	STORE	True (Active) level 0 to +5 Vdc. False level +2.5 Vdc to Vcc. Requires a pulse duration of ≥ 1 μs. When placed at a static true (logic low) the 33 storage registers will follow their data inputs.
28	MULTIPLEX RATE CONTROL	When connected to an external timing capacitor, it will allow the multiplexer M.V. to free-run between 2 kHz to 32 kHz, depending on the value of the capacitor. When connected to an external clock it will allow triggering of the M.V. (2 kHz to 32 kHz).
29	PT/NT	When placed at ground it configures the position outputs to 0 volts true (negative transistion). When left open or pulled up to Vcc configures the position outputs to Vcc true (position transistion).
30 31 32 33 34 35 36 37 38	POS1 POS2 POS4 POS3 POS6 Not Used POS5 POS8 POS7	Position outputs are negative true when pin 29 is at ground, and positive true when pin 29 is left open or pulled up to Vcc.
39	GND	Provides the ground return for the Vcc supply.
40	RESET	Will reset the six decade counters of the count chain and the over-flow detector, when placed at a logic low (0 Vdc to +0.5 Vdc) for a duration of ≥ 1 μs.

The SD057306 is a programmed SN74188A IC Read Only Memory that generates the Decimal Point and Measurement Unit data for the 63X1A series counters. The following table provides the SD057306 program.

BINARY SELECTS (ROM INPUTS)					SIX BIT OUTPUT ADDRESS (ROM OUTPUTS)					
A	B	C	D	E	Y1	Y2	Y3	Y4	Y5	Y6
0	0	0	0	0	1	0	0	1	1	0
0	0	0	1	0	0	1	0	1	1	0
0	0	1	0	0	1	1	0	1	1	0
0	0	1	1	0	0	0	1	1	1	0
0	1	0	0	0	1	0	0	1	1	0
0	1	0	1	0	0	1	0	1	1	0
0	1	1	0	0	1	1	0	1	1	0
0	1	1	1	0	0	0	1	1	1	0
1	0	0	0	0	1	0	0	1	1	0
1	0	0	1	0	0	1	0	1	1	0
1	0	1	0	0	1	1	0	1	1	0
1	0	1	1	0	0	0	1	1	1	0
1	1	0	0	0	1	0	0	1	1	0
1	1	0	1	0	0	1	0	1	1	0
1	1	1	0	0	1	1	0	1	1	0
1	1	1	1	0	0	0	1	1	1	0
0	0	0	0	1	0	1	0	1	0	1
0	1	0	0	1	1	0	0	1	0	1
1	0	1	0	1	0	0	0	1	0	1
1	1	1	0	1	0	1	0	0	1	1
0	0	0	1	1	0	1	0	1	0	1
0	1	0	1	1	1	0	0	1	0	1
1	0	1	1	1	0	0	0	1	0	1
1	1	1	1	1	0	1	0	0	1	1
0	0	0	0	1	0	1	0	1	0	1
0	1	0	0	1	1	0	0	1	0	1
1	0	1	0	1	0	0	0	1	0	1
1	1	1	0	1	0	1	0	0	1	1
0	0	0	1	1	0	1	0	1	0	1
0	1	0	1	1	1	0	0	1	0	1
1	0	1	1	1	0	0	0	1	0	1
1	1	1	1	1	0	1	0	0	1	1



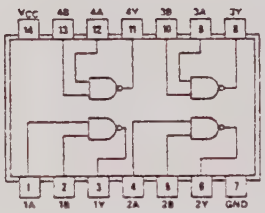
The SN74188A is a field-programmable, 256 bit, read-only memory organized as 32 words of eight bits each. This monolithic, high-speed, transistor-transistor-logic (TTL) memory array is addressed in five-bit binary with full on-chip decoding. An overriding memory-enable input is provided which, when taken high, will inhibit the function causing all eight outputs to remain high.

The address of an eight-bit word is accomplished through the buffered binary select inputs in coincidence with a low logic level at the enable input.

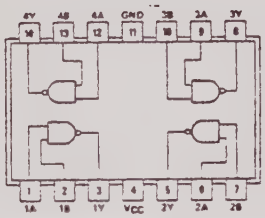
TTL LOW POWER SCHOTTKY QUAD 2-INPUT NAND GATES

SN7400N	S-D P/N 019705
SN74L00N	S-D P/N 025796
SN74LS00N	S-D P/N 103130
SN74S00N	S-D P/N 025785

positive logic:
$Y = \overline{AB}$



SN5400/SN7400(J, N)
SN54H00/SN74H00(J, N)
SN54L00/SN74L00(J, N)
SN54LS00/SN74LS00(J, N, W)
SN54S00/SN74S00(J, N, W)

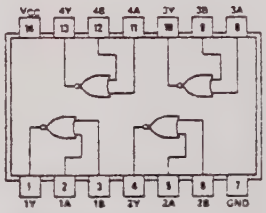


SN5400/SN7400(W)
SN54H00/SN74H00(W)
SN54L00/SN74L00(T)

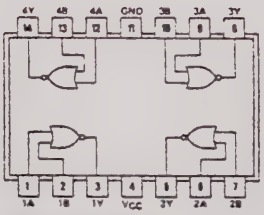
QUADRUPLE 2-INPUT POSITIVE-NOR GATES

SN7402N	S-D P/N 025709
SN74L02N	S-D P/N 025797
SN74LS02N	S-D P/N 103367

positive logic:
$Y = \overline{A+B}$



SN5402/SN7402(J, N)
SN54L02/SN74L02(J, N)
SN54LS02/SN74LS02(J, N, W)
SN54S02/SN74S02(J, N, W)



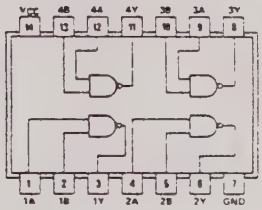
SN5402/SN7402(W)
SN54L02/SN74L02(T)

QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

SN7403N
SN74L03N

S-D P/N 103218
S- D P/N 045217

positive logic:
$Y = \overline{AB}$



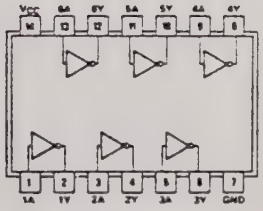
SN5403/SN7403(J, N)
SN54L03/SN74L03(J, N)
SN54LS03/SN74LS03(J, N, W)
SN54S03/SN74S03(J, N, W)

HEX INVERTERS

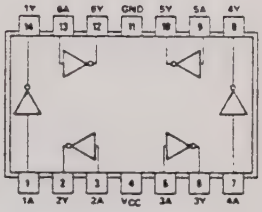
SN74H04N
SN74L04N
SN74LS04N

S-D P/N 106635
S-D P/N 045204
S-D P/N 103749

positive logic:
$Y = \overline{A}$



SN5404/SN7404(J, N)
SN54H04/SN74H04(J, N)
SN54L04/SN74L04(J, N)
SN54LS04/SN74LS04(J, N, W)
SN54S04/SN74S04(J, N, W)

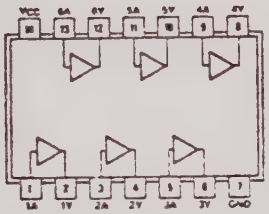


SN5404/SN7404(W)
SN54H04/SN74H04(W)
SN54L04/SN74L04(T)

HEX BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH VOLTAGE OUTPUTS

SN7407N — S-D P/N 045295

positive logic:
Y = A

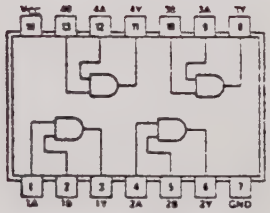


SN5407/SN7407(J, N, W)

TTL LOW POWER SCHOTTKY QUAD 2-INPUT AND GATES

SN7408N — S-D P/N 103093
SN74LS08N — S-D P/N 103967
SN74S08N — S-D P/N 117058

positive logic:
Y = AB



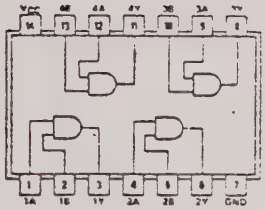
SN5408/SN7408(J, N, W)
SN54LS08/SN74LS08(J, N, W)

QUADRUPLE 2-INPUT POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

SN7409N

S-D P/N 103321

positive logic:
$Y = AB$

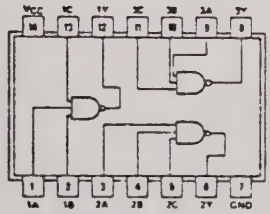


SN5409/SN7409(J, N, W)
SN54LS09/SN74LS09(J, N, W)

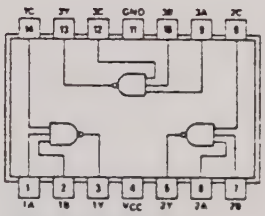
TRIPLE 3-INPUT POSITIVE-NAND GATES

SN7410N — S-D P/N 019706
SN74H10N — S-D P/N 025742
SN74L10N — S-D P/N 045218
SN74LS10N — S-D P/N 103968

positive logic:
$Y = \overline{ABC}$



SN5410/SN7410(J, N)
SN54H10/SN74H10(J, N)
SN54L10/SN74L10(J, N)
SN54LS10/SN74LS10(J, N, W)
SN54S10/SN74S10(J, N, W)



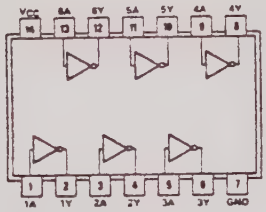
SN5410/SN7410(W)
SN54H10/SN74H10(W)
SN54L10/SN74L10(T)

HEX INVERTER BUFFERS/DRIVERS
WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

SN7416N

S-D P/N 045230

positive logic:
$Y = \overline{A}$



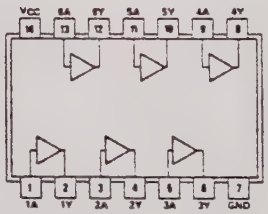
SN5416/SN7416(J, N, W)

TTL HEX BUFFER/DRIVER

SN7417N

S-D P/N 106629

positive logic:
Y = A

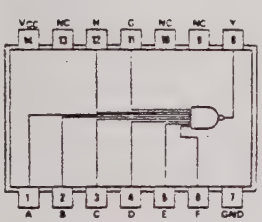


SN5417/SN7417(J, N, W)

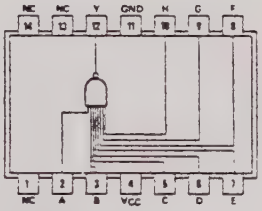
TTL LOW POWER SCHOTTKY 8-INPUT NAND GATE

SN7430N — S-D P/N 025726
SN74LS30N — S-D P/N 103971

positive logic:
$Y = \overline{ABCDEFGH}$



SN5430/SN7430(J, N)
SN54H30/SN74H30(J, N)
SN54L30/SN74L30(J, N)
SN54LS30/SN74LS30(J, N, W)
SN54S30/SN74S30(J, N, W)



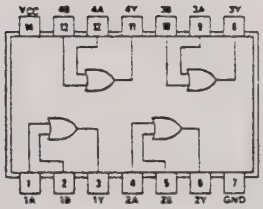
SN5430/SN7430(W)
SN54H30/SN74H30(W)
SN54L30/SN74L30(T)

NC—No internal connection

TTL QUAD 2-INPUT OR GATE

SN7432N — S-D P/N 045257
SN74LS32N — S-D P/N 103972
SN74S32N — S-D P/N 103973

positive logic:
Y = A+B



SN5432/SN7432(J, N, W)
SN54LS32/SN74LS32(J, N, W)

SN7490N

S-D P/N 025732

TRUTH TABLES

BCD COUNT SEQUENCE
(See Note 1)

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

RESET/COUNT (See Note 2)

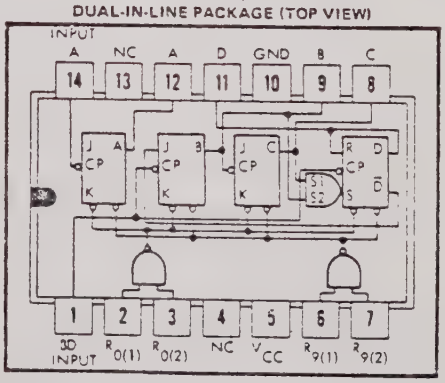
RESET INPUTS				OUTPUT
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	D C B A
1	1	0	X	0 0 0 0
1	1	X	0	0 0 0 0
X	X	1	1	1 0 0 1
X	0	X	0	COUNT
0	X	0	X	COUNT
0	X	X	0	COUNT
X	0	0	X	COUNT

NC—No Internal Connection

NOTES: 1. Output A connected to input BD for BCD count.
2. X indicates that either a logical 1 or a logical 0 may be present.

• Control Systems

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



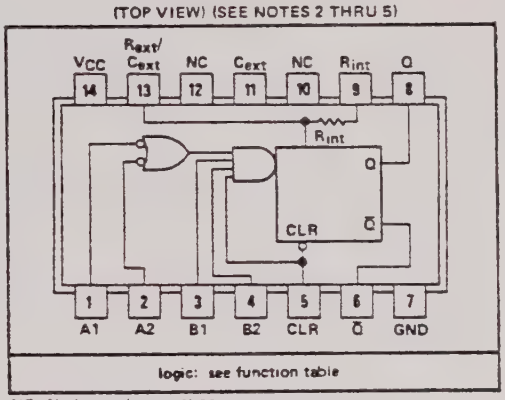
'LS122 FUNCTION TABLE
(SEE NOTE 1)

INPUTS					OUTPUTS	
CLEAR	A1	A2	B1	B2	Q	$\bar{Q}$
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	X	L	L	H
X	L	X	H	H	L	H
H	L	X	↑	H	⎍	⎎
H	L	X	H	↑	⎍	⎎
H	X	L	H	H	L	H
H	X	L	↑	H	⎍	⎎
H	X	L	H	↑	⎍	⎎
H	H	↓	H	H	⎍	⎎
H	↓	↓	H	H	⎍	⎎
H	↓	H	H	H	⎍	⎎
↑	L	X	H	H	⎍	⎎
↑	X	L	H	H	⎍	⎎

'LS123 FUNCTION TABLE
(SEE NOTE 1)

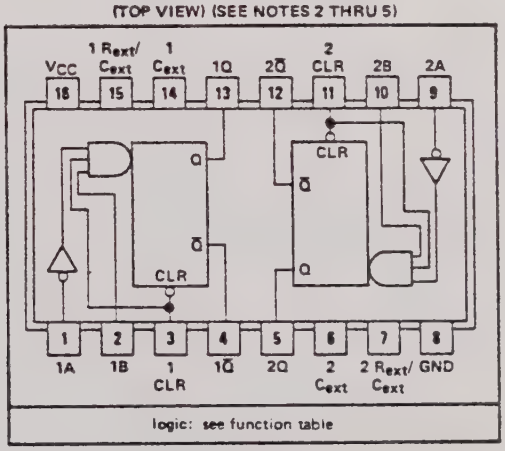
INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

SN54LS122 . . . J OR W PACKAGE
SN74LS122 . . . J OR N PACKAGE
(TOP VIEW) (SEE NOTES 2 THRU 5)



NC—No internal connection.

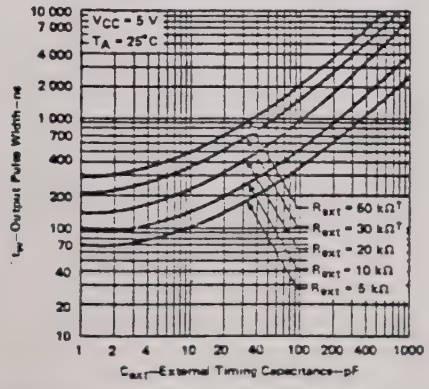
SN54LS123 . . . J OR W PACKAGE
SN74LS123 . . . J OR N PACKAGE
(TOP VIEW) (SEE NOTES 2 THRU 5)



description

The 'LS122 and 'LS123 multivibrators feature d-c triggering from gated low-level-active (A) and high-level-active (B) inputs, and also provide overriding direct clear inputs. Complementary outputs are provided. The retrigger capability simplifies the generation of output pulses of extremely long duration. By triggering the input before the output pulse is terminated, the output pulse may be extended. The overriding clear capability permits any output pulse to be terminated at a predetermined time independently of the timing components R and C. Enough Schmitt hysteresis is provided to ensure jitter-free triggering from the B inputs with transition rates as slow as 1 volt per second. Figure 1 illustrates triggering the one-shot with the high-level-active (B) inputs.

TYPICAL OUTPUT PULSE WIDTH
vs
EXTERNAL TIMING CAPACITANCE



SN74LS196N
SN74196N

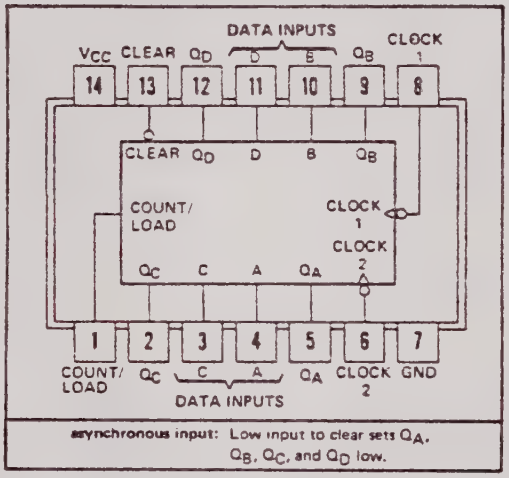
50/30 MHz PRESETTABLE DECADE OR BINARY COUNTERS/LATCHES

S-D P/N 103164
S-D P/N 025784

- Performs BCD, Bi-Quinary, or Binary Counting
- Fully Programmable
- Fully Independent Clear Input
- Input Clamping Diodes Simplify System Design
- Output Q_A Maintains Full Fan-out Capability In Addition to Driving Clock-2 Input

TYPES	GUARANTEED COUNT FREQUENCY CLOCK 1	GUARANTEED COUNT FREQUENCY CLOCK 2	TYPICAL POWER DISSIPATION
'196, '197	0-50 MHz	0-25 MHz	240 mW
'LS196, 'LS197	0-30 MHz	0-15 MHz	60 mW

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)


DATA INPUTS
VCC CLEAR QD D B QB CLOCK 1
14 13 12 11 10 9 8
CLEAR QD D B QB
COUNT/ LOAD
CLOCK 1
CLOCK 2
QC C A QA
1 2 3 4 5 6 7
COUNT/ LOAD QC C A QA CLOCK 2 GND
DATA INPUTS

asynchronous input: Low input to clear sets Q_A, Q_B, Q_C, and Q_D low.

description

These high-speed monolithic counters consist of four d-c coupled, master-slave flip-flops which are internally interconnected to provide either a divide-by-two and a divide-by-five counter ('196, 'LS196) or a divide-by-two and a divide-by-eight counter ('197, 'LS197). These four counters are fully programmable; that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independent of the state of the clocks.

During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. These counters feature a direct clear which when taken low sets all outputs low regardless of the states of the clocks.

These counters may also be used as 4-bit latches by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count/load is high and the clock inputs are inactive.

All inputs are diode-clamped to minimize transmission-line effects and simplify system design. These circuits are compatible with most TTL and DTL logic families. Typical power dissipation is 60 milliwatts. Series 54 and 54LS circuits are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74 and 74LS circuits are characterized for operation from 0°C to 70°C.

typical count configurations

'196 and 'LS196 typical count configurations and function tables are the same as those for '176. See page 370.
'197 and 'LS197 typical count configurations and function tables are the same as those for '177. See page 370.

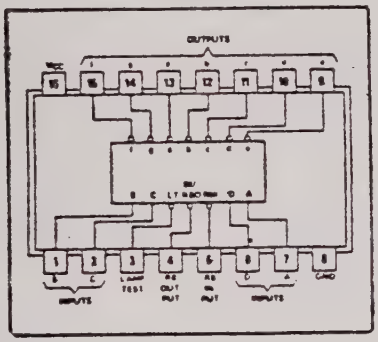
functional block diagrams

'196 and 'LS196 functional block diagram is the same as that for '176. See page 371.
'197 and 'LS197 functional block diagram is the same as that for '177. See page 371.

SN74247N
SN74LS247

S-D P/N 103314
S-D P/N 103166

'246, '247, 'LS247
(TOP VIEW)



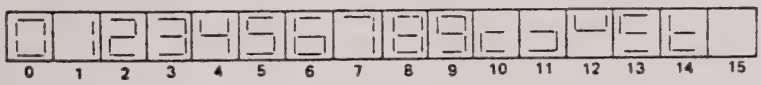
description

The '246 through '248 are electrically and functionally identical to the SN5446A/SN7446A, SN5447A/SN7447A, and SN5448/SN7448, respectively, and have the same pin assignments as their equivalents. Also the 'LS247 and 'LS248 are electrically and functionally identical to the SN54LS47/SN74LS47 and SN54LS48/SN74LS48, respectively, and have the same pin assignments as their equivalents. They can be used interchangeably in present or future designs to offer designers a choice between two indicator fonts. The '249 and 'LS249 are 16-pin versions of the 14-pin SN5449 and SN54LS49/SN74LS49, respectively. Included in the '249 and 'LS249 circuits is the full functional capability for lamp test and ripple blanking, which is not available in the '49 and 'LS49 circuits. The '46A, '47A, '48, '49, 'LS47, 'LS48, and 'LS49 compose the 6 and the 9 without tails and the '246 through '249 and 'LS247, 'LS248, and 'LS249 compose the 6 and the 9 with tails. Composition of all other characters, including display patterns for BCD inputs above nine, is identical. The '246, '247, and 'LS247 feature active-low outputs designed for driving indicators directly, and the '248, '249, 'LS248, and 'LS249 feature active-high outputs for driving lamp buffers. All of the circuits have full ripple-blanking input/output controls and a lamp test input. Segment identification and resultant displays are shown below. Display patterns for BCD input counts above 9 are unique symbols to authenticate input conditions.

All of these circuits incorporate automatic leading and/or trailing-edge zero-blanking control (RBI and RBO). Lamp test (LT) of these types may be performed at any time when the BI/RBO node is at a high level. All types contain an overriding blanking input (BI) which can be used to control the lamp intensity by pulsing or to inhibit the outputs. Inputs and outputs are entirely compatible for use with TTL or DTL logic outputs.

Series 54 and Series 54LS devices are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74 and Series 74LS devices are characterized for operation from 0°C to 70°C.

SEGMENT IDENTIFICATION



NUMERICAL DESIGNATIONS AND RESULTANT DISPLAYS

CHAPTER 6

REPLACEABLE PARTS

6.1 INTRODUCTION

This chapter contains the spare parts lists for each assembly in the Model 63X1A Counter Timers. Chapter 7 shows the assemblies where the listed parts are installed. Ordering information is included and should be used when purchasing parts from the factory. Explanation of the column listings and Table 6.1 Manufacturers Code-To-Name Index are also included.

6.2 PART ORDERING INFORMATION

To order a part from the Replaceable Parts List, state the Systron-Donner part number, indicate the quantity required and address the order to the nearest Systron-Donner sales or service center.

To order a part not listed in the Replaceable Parts List, state the instrument model number, instrument serial number, the description and function of the part, and the number of parts required. Address the order to the nearest Systron-Donner sales or service center.

6.3 PARTS LISTS

Table 6.1 gives the code-to-name information for the manufacturers listed in the replaceable parts lists. The replaceable parts lists are placed in a numbered sequence.

Each column in the parts lists provide specific information relating to the listed parts as follows:

(1) DESIGNATOR: Reference numbers applicable to assemblies are listed in alpha-numeric order.

(2) COMPONENT NOMENCLATURE AND DESCRIPTION: Component names and specifications are provided in these columns and include; values, tolerance, wattage rating, working voltage, construction, etc.

(3) MANUFACTURER'S CODE: H4-2 Federal Supply Code numbers are listed to identify component manufacturers. A Manufacturers Index is provided in this chapter for cross-reference.

(4) MANUFACTURER'S PART NUMBER: True manufacturer part numbers are listed in this column.

(5) SD STOCK NUMBER: The Systron-Donner stock number is listed in this column.

(6) T/Q (Total Quantity): This quantity, appearing after an item entry, indicates the number of times the component is used in that assembly. The total quantity for each part is given only once - at the first appearance of the part number in the list.

REPLACEABLE PARTS LIST

TITLE		FINAL ASSEMBLY Model 63X1A				
ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
		ASSEMBLY Test Model 6341A	52542	057839	057839	1
		ASSEMBLY Test Model 6351A	52542	057836	057836	1
		ASSEMBLY Test Model 6361A	52542	057833	057833	1
		COVER, Top	52542	057260	057260	1
		COVER, Bottom	52542	057261	057261	1
		EXTENDER, Cover	52542	057694	057694	2
		FOOT BAIL	52542	057064	057064	4
		BAIL	52542	057132	057132	1
		BUMPER, Rubber	77969	4460	103880	4
		LINE CORD	70903	BR-1736	102407	1
		SCREW, PHMS 6-32 x 1/2	96906	MS51957-30	10063208	2
		SCREW, PH 6-32 x 5/8	96906	MS51957-31	10063210	4
		SCREW, 6-32 x 3 1/2	96906		10063256	4
		NUT, Hex 6-32 Small Pattern	96906	NAS671C6	100638	4
		WASHER, #6 Int. Tooth	96906	MS35333-71	100647	6
		OPTION 35 BCD 6341A & 6351A	52542	057928	057928	1
		OPTION 35 BCD 6361A only	52542	057927	057927	1

TITLE		MODEL 63X1A TEST ASSEMBLY #057833 Figure 7-1				
ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
1		ASSEMBLY, Universal	52542	057831	057831	1
2		ASSEMBLY, Front Panel (6341A)	52542	057838	057838	1
2		ASSEMBLY, Front Panel (6351A)	52542	057835	057835	1
2		ASSEMBLY, Front Panel (6361A)	52542	057832	057832	1
3	A2	ASSEMBLY, 100 MHz Amp Right	52542	057720	057720	1
4	A4	ASSEMBLY, 100 MHz Amp Left (except 6341A)	52542	057721	057721	1
5	A3	ASSEMBLY, Decade PC	52542	05745701	05745701	1
5	A5	ASSEMBLY, Decade PC (6361A only)	52542	05745701	05745701	1
6		KNOB	07933	50-1WD-1G	103371	2
7		SCREW, 4-40 x 5/16 PHMS	96906	MS51957-14	10062605	2
8		WASHER, #6 flat	86928	5710-23-10	100662	2
9		WASHER #6 split	96906	MS35338-136	100712	
		Model 6341A				6
		Model 6351A				8
		Model 6361A				10
10	W1	JUMPER, Molded (except 6361A)	Gettig	L-2007-1	102879	1
11		SCREW, 6-32 x 5/16 PHMS	96906	MS51957-27	10063205	
		Model 6341A				6
		Model 6351A				8
		Model 6361A				10

REPLACEABLE PARTS LIST

TITLE	UNIVERSAL ASSEMBLY #057831 Figure 7-4				
ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
1		ASSEMBLY, Rear Panel	52542	057736	057736	1
2		ASSEMBLY, Mother Board PC	52542	05747401	05747401	1
4		SCREW 6-32 x 5/16 PHMS	96906	MS51957-27	10063205	4
5		WASHER, #6 Split	96906	MS35338-136	100712	4
6		ASSEMBLY, 10 MHz Osc. PC	52542	05708801	05708801	1
7		WASHER, #6 Flat	86928	5710-23-10	100662	2

TITLE: FRONT PANEL ASSEMBLY Model 63X1A #057832 Figure 7-2

ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
1		SUB PANEL	52542	057456	057456	1
2		DECORATIVE PANEL Model 6341A	52542	057601	057601	1
2		DECORATIVE PANEL Model 6351A	52542	057602	057602	1
2		DECORATIVE PANEL Model 6361A	52542	057603	057603	1
3		PANEL ASSEMBLY Hold Down	52542	057680	057680	2
4		DISPLAY PC Assembly Model 6341A	52542	05747503	05747503	1
4		DISPLAY PC Assembly Model 6351A	52542	05747502	05747502	1
4		DISPLAY PC Assembly Model 6361A	52542	05747501	05747501	1
5		SPACER #4 x 3/16L	06540	9208N-115	101077	4
6		SCREW 4-40 x 1 1/4	96906	MS51957-22	10062620	4
7		WASHER #4 Split	96906	MS35338-135	100711	4
10	S1	SWITCH PB W/ Dressnut	81073	30-3 W/Dressnut	102347	1
8	S2	SWITCH Toggle SPDT W/Dressnut	09353	7101PN + Dressnut	102346	1
9	S3	SWITCH Toggle 4 PDT	09353	7401	102337	1
	S4	Not Used				
8	S5	SWITCH Toggle SPDT W/Dressnut (Model 6361A only)	09353	7101 PN + Dressnut	102346	1
10	S6	SWITCH PB W/Dressnut	81073	30-3 W/Dressnut	102347	1
11		DRESSNUT, Black (for item 9)	09353	B7099N	101086	1

REPLACEABLE PARTS LIST

TITLE	REAR PANEL ASSEMBLY #057736 Figure 7-3					
ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
1		REAR PANEL	52542	057429	057429	1
7	C101 thru C104	CAPACITOR, Tant 1μF 35V 10%	56289	150D105X9035A2	100082	4
10	F1	FUSE, 1A Slo Blo 250V	75915	313001	100584	1
6	J1, J2	BNC Connector Front Mtd	96906	UG-1094/U	101155	2
	J3	AC Receptacle	82389	EAC-301	101288	1
4		COVER PLATE	52542	057655	057655	2
3		END BELL	52542	10367701	10367701	1
8	S4	SWITCH, Toggle SPDT	09353	7101	102310	1
9	XF1	FUSE POST	75915	342004	102409	1
12	U101	IC, Voltage Regulator	27014	LM345K	117259	1
11	U102	IC, Voltage Regulator	27014	LM323K	117258	1
13		INSULATOR To-3 Cover	Jermyn	A22-4015	102965	1
14		WASHER, Nylon Shoulder	83330	2661	102868	2
15		BNC Ground Lug	79963	814	107077	2
16		INSULATOR To-3 Mica	08289	DM-103	102940	1
17		NUT 4-40, Hex	96906	NAS671C4	100622	4
18		WASHER #4 Split	96906	MS35338-135	100711	4
19		SCREW, 4-40 x 1/2 PH	96906	MS51957-17	10062608	2
20		WASHER, #4 flat	96906	MS15795-803	100703	6
21		WASHER, #2 split	96906	MS35337-77	100661	4
22		SCREW, 2-56 x 3/16 PH	96906	MS51957-2	10062503	4
23		SCREW, 8-32 x 1 1/2 PH	96906	MS51957-51	10064224	4
24		WASHER #8 flat	86928	5702-225-30-C1	103014	4
25		NUT 8-32 KEP	78189	511-081800-00	100940	4
26		SCREW, 4-40 x 7/16 PH	96906	MS51957-16	10062607	2
27		SCREW, 4-40 x 5/16 PH	96906	MS51957-14	10062605	2
28		SCREW, 6-32 x 3/8 PH	96906	MS51957-28	10063206	2
29		NUT, Hex 6-32 Sml Pat	96906	NAS671C6	100638	2
30		SOLDER LUG #6	83330	1413-6	100486	1
31		SOLDER LUG #4	83330	1416-4	100509	2
32		WASHER, #6 Split	96906	MS35338-136	100712	1

REPLACEABLE PARTS LIST

TITLE	MOTHER PC BOARD ASSEMBLY #05747401 Figure 7-5				
ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
		MOTHER BOARD	52542	057474	057474	1
	C1 thru C3	CAPACITOR, Cer .1 μF 50V 20%	56289	5C023104X0500C5	100178	5
	C4 thru C7	CAPACITOR, Dip Mica 100 pF 500V 5%	72136	DM15FD101JO	100173	3
	C8	Same as C1				
	C9	CAPACITOR, El 5000 μF 15V	99392	23C15TS53	106459	2
	C10	CAPACITOR, Cer .001 μF 1kV 20%	91418	Type B	100076	1
	C11	CAPACITOR, Cer .05 μF 10V +80-20%	71590	UK10-503	100122	14
	C12	Same as C9				
	C13	Same as C11				
	C14	Same as C11				
	C15	CAPACITOR, El 1500 μF 50V	99392	23C50TS152	106468	2
	C16	Same as C11				
	C17	Same as C11				
	C18	Same as C15				
	C19	Same as C11				
	C20	Same as C11				
	C21	CAPACITOR, Tant 39 μF 10V 10%	56289	150D396X9010B2	100183	2
	C22 thru C28	Same as C11				
	C29	CAPACITOR, El 100 μF 25V	56289	B41283-B5107-T	100165	1
	C30	CAPACITOR, 200 μF 35V +100-10%	90201	MTV200DN35	100308	1
	C31	Same as C21				
	CR1	DIODE, Sgnl 20V 2.69V Fwd	03508	1N4830	100440	1
	CR2	DIODE, Cap 27 pF	04713	MV2103	100433	1
	CR3	DIODE, Rect 50V Ld Temp	81483	30S05	103252	4
	CR4 thru CR6	Same as CR3				
	CR7	DIODE, Rect 600V 1A	04713	1N4005	100413	4
	CR8 thru CR10	Same as CR7				
	L1	INDUCTOR .15 μH 10%	72259	DD-0.15	101311	2
	L2	Same as L1				
	Q1	TRANSISTOR, SIPNP 12V	07263	PN3640-18	101357	1
	Q2	TRANSISTOR, SINPN 15V	07293	2N4275-18	102716	2
	Q3	Same as Q2				
	R1	RESISTOR, 12k 1/4W 5%	01121	CB1235	101565	3
	R2	RESISTOR, 470Ω 1/4W 5%	01121	CB4715	101625	3

REPLACEABLE PARTS LIST

TITLE: MOTHER PC BOARD ASSEMBLY (Cont)

ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/O
	R3	RESISTOR, 10k 1/4W 5%	01121	CB1035	101570	1
	R4	Same as R2				
	R5	Same as R2				
	R6	RESISTOR, 3.3k 1/4W 5%	01121	CB3325	101559	2
	R7	Same as R6				
	R8	RESISTOR, 130Ω 1/4W 5%	01121	CB1315	101627	3
	R9	RESISTOR, 560Ω 1/4W 5%	01121	CB5615	101583	7
	R10	Same as R9				
	R11	RESISTOR, 2.2k 1/4W 5%	01121	CB2225	101562	4
	R12	Same as R11				
	R13	RESISTOR, 1k 1/4W 5%	01121	CB1025	101569	2
	R14	Same as R9				
	R15	RESISTOR, 150Ω 1/4W 5%	01121	CB1515	101615	1
	R16	Same as R11				
	R17	Same as R11				
	R18	Same as R13				
	R19	RESISTOR, 27Ω 1/4W 5%	01121	CB2705	101729	1
	R20 thru R23	Same as R9				
	R25 thru R44	RESISTOR, 47k 1/4W 5%	01121	CB4735	101574	20
	R45	RESISTOR, 1.5k 1/4W 5%	01121	CB1525	101577	2
	R46	Same as R45				
	R47	Same as R8				
	R48	Same as R8				
	R49	RESISTOR, 82Ω 1/4W 5%	01121	CB8205	101629	3
	R50	Same as R49				
	R51	Same as R1				
	R52	Same as R49				
	U1	IC, TTL Hex Inv 15V	01295	SN7416N	045230	1
	U2	IC, TTL Quad 2-In AND	01295	SN74LS08N	103967	1
	U3	IC, TTL Hex Buffer 15V	01295	SN7417N	106629	1
	U4	IC, TTL Quad 2-In NAND	01295	SN74LS00N	103130	2
	U5	IC, ECL Quad 2-In NOR	04713	MC10102P	103025	2
	U6	IC, ECL Quad Gate	04713	MC10101L	025791	1
	U7	Same as U5				
	U8	IC, Quad TTL/ECL	04713	MC10124	045228	1
	U9	IC, TTL 3 3-In NAND	01295	SN74LS10N	103968	1
	U10	IC, ECL Emitter Coup Osc	04713	MC1648P	045236	1
	U11	IC, ECL MSI 100 MHz	04713	MC10138P	103837	1
	U12	IC, TTL 8-In NAND	01295	SN74LS30N	103971	1

TITLE		MOTHER PC BOARD ASSEMBLY (Cont)				
ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
	U13	IC, TTL 4 2-In OR	01295	SN74LS32N	103972	3
	U14	Same as U13				
	U15	IC, TTL MSI Dec Ctr	01295	SN7490N	025732	8
	U16	Same as U15				
	U17	Same as U15				
	U18	Same as U4				
	U19	IC, Op Amp	02735	CA3130T	103231	1
	U20	IC, ECL Phase-Freq. Det.	04713	MC12040P	045277	1
	U21 thru U25	Same as U15				
	U26 thru U31	IC, Res Mod 4 - 12k 1W 20%	52542	045008	045008	6
	U32	Same as U13				
		CONNECTOR, 5 pos. Plug Shell	27264	03-06-2055	101263	2
		CONNECTOR, Term Male PC	27264	02-06-8103	10282203	10
		CONNECTOR, 72 Pin PC	30146	929853	117177	2
		CONNECTOR, Cual 36 Pin PC	05574	3VH36/1CV12	103316	1
		TERMINAL, Swage	88245	2000B	100482	7
		BLOCK Swage 6-32	88245	1590B	100489	2
		SPACER Swage 6-32 x 1/8	88245	1530B 1/8	100478	8
		SPACER Swage 6-32 x 1/4	71279	1247-11	100539	2

REPLACEABLE PARTS LIST

TITLE A1, DISPLAY PC ASSEMBLY (Figure 7-9, 7-10 & 7-11)

ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
	A1	ASSEMBLY, PC Display Model 6341A	52542	05747503	05747503	Ref
	A1	ASSEMBLY, PC Display Model 6351A	52542	05747502	05747502	Ref
	A1	ASSEMBLY, PC Display Model 6361A	52542	05747501	05747501	Ref
	DS1 thru DS8	DISPLAY, 7 Seg. Same Color Dot	50522	MAN4610A	10317201	8
	DS9 thru DS13	DISPLAY, Led Amber	50522	5152	103936	5
	DS14 thru DS21	Same as DS1 (6361A only)	50522	MAN4610A	10317201	8
	DS22 thru DS26	Same as DS9 (6361A only)	50522	5152	103936	5
	Q1 thru Q8	TRANSISTOR, SIPNP	04713	MPSA63	117349	8
	Q9	TRANSISTOR, SINPN	04713	MPSA12	101396	2
	Q10	Same as Q9				
	Q11 thru Q18	Same as Q1 (6361A only)	04713	MPSA63	117349	8
	Q19, Q20	Same as Q9 (6361A only)	04713	MPSA12	101396	2
	R1 thru R8	RESISTOR, 27Ω 1/4W 5%	01121	CB2705	101729	8
	R9 thru R13	RESISTOR, 150Ω 1/4W 5%	01121	CB1515	101615	5
	R14 thru R21	Same as R1 (6361A only)	01121	CB2705	101729	8
	R22 thru R26	Same as R9 (6361A only)	01121	CB1515	101615	5
	S1 thru S4	SWITCH, 4 Pos P.B. Assy. (6361A only)	52542	057577	057577	4
	S2 thru S4	SWITCH, 4 Pos P.B. (6341A & 6351A)	52542	057577	057577	3
	U1	IC, TTL, MSI BCD 7 Seg Dcd/Drvr	01295	SN74247N	103314	1
	U2	Same as U1 (6361A only)				
	XDS1 thru XDS8	SOCKET, 14 Pin Dip Wire Wrap	73803	C91-14-00	102928	8
	XD14 thru XD21	Same as XDS1 (6361A only)	73803	C91-14-00	102928	8

REPLACEABLE PARTS LIST

TITLE	A2, 100 MHz AMPLIFIER RIGHT ASSEMBLY #057720 Figure 7-13					
ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
1		ASSEMBLY, 100 MHz Amp PC	52542	05747701	05747701	1
2		SHIELD, Amplifier Right	52542	05764801	05764801	1
3		SPACER, Swage 6-32 x 1/2	88245	1530 B 1/2	100532	4
4		SPACER, BNC	52542	A045062	045062	1
5	J1	CONNECTOR, BNC	96906	UG-1094A/U	101170	1
6		LUG, BNC Gnd	79963	334-375	112551	1
13	S1	SWITCH SPDT Toggle	09353	7101PN+Dressnut	102346	1
7	S2	SWITCH Pushbutton	52542	057722	057722	1
12	S3/R01	SWITCH, Panel Pot 10k 10%	80294	86C2A-E20-A15/R	117264	1
13	S4	Same as S1				
8		BRACKET Mounting	79963	176	100849	2
9	R1, R6	RESISTOR, 909k 1%	19701	MF5C-D-9093-F	102159	2
10	CR101	DIODE, Led Red	28480	HPA 5082-4480	100460	1
15		WASHER #6 Flat	86928	5710-23-10	100662	6
16		WASHER #6 Split	96906	MS35338-136	100712	6
17		WASHER #2 Split	96906	MS35337-77	100661	2
18		NUT, Hex #2-56	96906	MS35649-224	100636	2
20		SCREW, 6-32 x 1/4 PHMS	96906	MS51957-26	10063204	6
21		SCREW, 2-56 x 1/4 PHMS	96906	MS51957-3	10062504	2
23		CABLE ASSEMBLY	52542	057718	057718	1

REPLACEABLE PARTS LIST

TITLE	A4, 100 MHz AMPLIFIER LEFT ASSEMBLY #057721 Figure 7-14				
ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
1		ASSEMBLY, 100 MHz Amp PC	52542	05747701	05747701	1
2		SHIELD, Amplifier Left	52542	05764802	05764802	1
3		SPACER, Swage 6-32 x 1/2	88245	1530 B 1/2	100532	4
4		SPACER, BNC	52542	A045062	045062	1
5	J1	CONNECTOR, BNC	96906	UG-1094A/U	101170	1
6		LUG, BNC Gnd	79963	334-375	112551	1
13	S1	SWITCH SPDT Toggle	09353	7101PN+Dressnut	102346	1
7	S2	SWITCH, Pushbutton	52542	057722	057722	1
12	S3/R01	SWITCH, Panel Pot 10k 10%	80294	86C2A-E20-A15/R	117264	1
13	S4	Same as S1				
8		BRACKET Mounting	79963	176	100849	2
9	R1, R6	RESISTOR, 909k 1%	19701	MF5C-D-9093-F	102159	2
10	CR101	DIODE, Led Red	28480	HPA 5082-4480	100460	1
15		WASHER #6 Flat	86928	5710-23-10	100662	6
16		WASHER #6 Split	96906	MS35338-136	100712	6
17		WASHER #2 Split	96906	MS35337-77	100661	2
18		NUT, Hex #2-56	96906	MS35649-224	100636	2
20		SCREW, 6-32 x 1/4 PHMS	96906	MS51957-26	10063204	6
21		SCREW, 2-56 x 1/4 PHMS	96906	MS51957-3	10062504	2
23		CABLE ASSEMBLY	52542	057718	057718	1

TITLE	A2 & A4 100 MHz AMPLIFIER PC ASSEMBLY #05747701 Figure 7-15				
ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
		PC BOARD	52542	057477	057477	1
	C1	CAPACITOR, .1 μF chip 500V	29454	501S48W104PPS	103755	1
	C2	CAPACITOR, DM 7 pF 500V 1%	14655	CD6CD070D03	106405	2
	C3	CAPACITOR, DM 60 pF 500V 1%	72136	DM15FD600FO	100324	2
	C4	Same as C3				
	C5	Same as C2				
	C6	CAPACITOR, CM 47 pF 500V 5%	72136	DM15ED470JO	100171	1
	C7	CAPACITOR, Cer Disc .001 μF 1kV 20%	91418	Type B	100076	7
	C8	CAPACITOR, Varcer 15-60 pF 200V	72982	538-006, F15-60	106502	1
	C9 thru C13	Same as C7				
	C14	CAPACITOR, Cer .05 μF 10V +80-20%	71590	UK10-503	100122	3
	C15	CAPACITOR, Tant 1 μF 35V 10%	56289	150D105X9035A2	100082	4
	C16 thru C18	Same as C15				
	C19	Same as C14				
	C20	Same as C14				
	C21	CAPACITOR, 100 μF 10V 10%	56289	196D107X9010PA1	103714	2
	C22	Same as C7				
	C23	Same as C21				
	CR1	DIODE, Zener 5% .4W	04713	1N958B	102992	2
	CR2	DIODE, Signal	52542	SD037769	037769	2
	CR3	Same as CR2				
	CR4	Same as CR1				
	CR5	DIODE, Signal 50V	03508	1N4151	100385	2
	CR6	Same as CR5				
	CR7	DIODE, Ref 6.2V 5%	04713	1N823B	720461	2
	CR8	Same as CR7				
	CR9	DIODE, Signal 20V	28480	HP5082-2810	103346	2
	CR10	Same as CR9				
	CR101	P/O A2 and A4 Assembly				
	Q1	TRANSISTOR, JFET N Chnl	17856	2N5564	117184	1
	Q2	TRANSISTOR, SIPNP 20V	04713	MPS-H81	117263	4
	Q3 thru Q5	Same as Q2				

REPLACEABLE PARTS LIST

TITLE: A2 & A4 100 MHz AMPLIFIER PC ASSEMBLY (Cont)

ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
	R1	P/O A2 and A4 Assembly				
	R2	RESISTOR, 117k MF 1/2%	83781	RTS-41	103422	1
	R3	RESISTOR, 39Ω 1/4W 5%	01121	CB3905	101733	2
	R4	Same as R3				
	R5	RESISTOR, MF 102k .12W 1%	81349	RN60C1023F	106207	3
	R6	P/O A2 and A4 Assembly				
	R7	RESISTOR, 4.7k 1/4W 5%	01121	CB4725	101598	2
	R8	Same as R5				
	R9	Same as R7				
	R10	RESISTOR, MF 1k .12W 1%	81349	RN60C1001F	106161	2
	R11	RESISTOR, MF 10k .12W 1%	81349	RN60C1002F	106162	2
	R12	Same as R11				
	R13	Same as R10				
	R14	RESISTOR, MF 5.62k .12W 1%	81349	RN60C5621F	106194	2
	R15	RESISTOR, MF 221Ω .1W 1%	81349	RN55D2210F	102065	2
	R16	Same as R15				
	R17	RESISTOR, CC 3.3k 1/4W 5%	01121	CB3325	101559	1
	R18	RESISTOR, CC 100Ω 1/4W 5%	01121	CB1015	101609	1
	R19	RESISTOR, Variable 1k 15T PC	73138	89PR1K	102181	1
	R20	RESISTOR, Variable 2k 15T PC	73138	89PR2K	102119	1
	R21	RESISTOR, MF 1.27k .12W 1%	91637	MFF 1/8 T1	102237	2
	R22	RESISTOR, CC 560Ω 1/4W 5%	01121	CB5615	101583	9
	R23	Same as R21				
	R24	RESISTOR, CC 22Ω 1/4W 5%	01121	CB2205	101696	2
	R25	Same as R24				
	R26	Same as R14				
	R27	Same as R5				
	R28	RESISTOR, CC 1k 1/4W 5%	01121	CB1025	101569	2
	R29	Same as R22				
	R30	Same as R28				
	R31	RESISTOR, MF 2.74k .12W 1%	81349	RN60C2781F	106178	2
	R32	Same as R31				
	R33	Same as R22				
	R34	RESISTOR, CC 470Ω 1/4W 5%	01121	CB4715	101625	4
	R35	Same as R34				
	R36	RESISTOR, CC 51Ω 1/4W 5%	01121	CB5105	101672	2
	R37	Same as R36				
	R38	Same as R22				
	R39	Same as R34				
	R40	Same as R34				

TITLE: A2 & A4 100 MHz AMPLIFIER PC ASSEMBLY (Cont)

ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
	R41	Same as R22				
	R42	Same as R22				
	R43	RESISTOR, 68Ω 1/4W 5%	01121	CB6805	101690	2
	R44	Same as R43				
	R45	RESISTOR, CC 220Ω 1/4W 5%	01121	CB2215	101566	3
	R46	Same as R45				
	R47	Same as R22				
	R48	Same as R22				
	R49	RESISTOR, CC 5.6k 1/4W 5%	01121	CB5625	101584	3
	R50	Same as R49				
	R51	Same as R49				
	R52	Same as R22				
	R53	RESISTOR 150Ω 1/8W 5%	01121	BB1515	101702	2
	R54	Same as R53				
	R55	RESISTOR, CC 100k 1/4W 5%	01121	CB1045	101558	3
	R56	Same as R55				
	R57	Same as R55				
	R58	RESISTOR, CC 1.2k 1/4W 5%	01121	CB1225	101581	2
	R59	Same as R45				
	R60	Same as R58				
	R61	RESISTOR, CC 390Ω 1/4W 5%	01121	GB1035	101592	1
	R62	RESISTOR, Variable 5k 1T PC	73138	72XL R5K	117124	1
	R101	P/O A2 and A4 Assembly				
	U1	IC, ECL Quad 2-In NOR	04713	MC10102P	103025	1
	U2	IC, ECL Triple Line Rcvr	04713	MC10216L	045276	1
	U3	IC, Lin MSC NPN	02735	CA3018	025720	1
	U4	IC, Volt Reg	04713	MC79L15ACP	117261	1
	U5	IC, Volt Reg	04713	MC78L15ACP	117260	1
		WASHER, Nylon Flat	86928	5610-120-31	117279	1
	TP1/TP2	Feed Thru Test Point	98921	001-1007	100575	2

TITLE A3, A5 DECADE PC ASSEMBLY #05745701 Figure 7-18

ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
		DECADE PC BOARD	52542	057457	057457	Ref
	C1	CAPACITOR, Tant 22 μF 15V 10%	56289	150D226X9015B2	100125	1
	C2	CAPACITOR, Cer Disc .001 μF 1 kV 20%	91418	Type B	100076	5
	C3	CAPACITOR, Tant 1 μF 35V 10%	56289	150D105X9035A2	100082	1
	C4	Same as C2				
	C5	CAPACITOR, Tant 2.2 μF 20V 10%	56289	150D225X9020A2	100203	1
	C6	CAPACITOR, Cer .05 μF 10V +80-20%	71590	UK10-503	100122	7
	C7	Same as C6				
	C8	Same as C6				
	C9	CAPACITOR, Tant 39 μF 10V 10%	56289	150D396X9010B2	100183	2
	C10 thru C13	Same as C6				
	C14	Same as C9				
	C15 thru C17	Same as C2				
	CR1 thru CR2	DIODE, Signal 50V	03508	1N4151	100385	2
	P1	CONNECTOR, 72 Pin	30146	929838-01-36	117179	1
	Q1	TRANSISTOR, SIPNP 12V	07263	2N3640	101357	1
	R1	RESISTOR, 1k 1/4W 5%	01121	CB1025	101569	3
	R2	Same as R1				
	R3	RESISTOR, 470Ω 1/4W 5%	01121	CB4715	101625	2
	R4	RESISTOR, 22k 1/4W 5%	01121	CB2235	101572	2
	R5	Same as R1				
	R6	RESISTOR, 10Ω 1/4W 5%	01121	CB1005	101557	1
	R7	RESISTOR, 100k 1/4W 5%	01121	CB1045	101558	1
	R8	Same as R4				
	R9	Same as R3				
	R10	RESISTOR, 4.7k 1/4W 5%	01121	CB4725	101598	2
	R11	Same as R10				
	R12	RESISTOR, 12k 1/4W 5%	01121	CB1235	101565	1
	U1	IC, TTL SSI Hex Inverter	01295	SN74LS04N	103749	1
	U2	IC, ECL 10k Mecl Trans	04713	MC10125	106660	2
	U3	IC, Quad 2-In NOR	04713	MC10102P	103025	1
	U4	IC, TTL SSI 4 2-In AND	01295	SN74LS08N	103967	1
	U5	IC, ECL MSI	04713	MC10138P	103837	1
	U6	IC, ECL Dual D M-S Flip-Flop	04713	MC10231L	045227	1
	U7	IC, TTL SSI Dual Retrig 1 Shot	01295	SN74LS123N	103976	1
	U8	Same as U2				

TITLE A3, A5 DECADE PC ASSEMBLY Figure 7-18 (Cont)

ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
	U9	IC, ECL SSI 4 2-In NOR	04713	MC10100P	103712	1
	U10	IC, TTL MSI Prst BCD Cntr	01295	SN74LS196N	103164	1
	U11	IC, TTL SSI 4 2-In NOR	01295	SN74LS32N	103972	1
	U12	IC, CMOS LSI Cnt Chain	52542	SD055095	055095	1
	U13	IC, LIN MSC Timer Wide Range	18324	NE555V	045208	1
	U14	IC, TTL ROM	52542	SD057306	057306	1
	U15	IC, CMOS SS Inv Buf	04713	MC14050BP	103492	1
	U16	IC, Res Mod 4 x 12k .1W 20%	52542	045008	045008	4
	U17	Same as U16				
	U18	IC, Res Mod 4 x 560Ω 20%	52542	055066	055066	1
	U19	Same as U16				
	U20	Same as U16				
	XU12	SOCKET, 40 Pin	73803	C83-40-02	117159	1
		BRACKET, Angle	79963	176	100849	2
		SCREW, PHMS 6-32 x 1/4	96906	MS51957-26	10063204	2
		WASHER #6 Flat	86928	5710-23-10	100662	2
		WASHER #6 Split	96906	MS35338-136	100712	2

REPLACEABLE PARTS LIST

TITLE	10 MHz OSCILLATOR PC ASSEMBLY #05708801 Figure 7-19				
ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
		PC Detail, 10 MHz Oscillator	52542	057088	057088	1
	C1	CAPACITOR, 9-35 pF	72982	538-006D9.0-35	100159	1
	C2	CAPACITOR, 15-60 pF	72982	538-011F15-60	100234	1
	C3	CAPACITOR, DM 150 pF 5% 500V	72136	DM15FD151JO	100219	1
	C4	CAPACITOR, 100 pF 5% 500V	72136	DM15FD101JO	10017301	1
	C5	CAPACITOR, DM 220 pF 5% 500V	72136	DM15FD221JO	10022001	1
	C6	CAPACITOR, 33 pF 5% 500V	72136	DM15ED330JO	10017501	1
	C7	CAPACITOR, DM 10 pF 5% 500V	72136	DM15CD100JO	10025301	1
	C8	CAPACITOR, Disc .01 µF	91418	TA110	100103	1
	C9	CAPACITOR, .05 µF 100V +80-20%	71590	UK10-503	100122	2
	C10	Same as C9				
	Q1	TRANSISTOR, SINPN 15V	07293	PN4275-18	102716	3
	Q2	Same as Q1				
	Q3	Same as Q1				
	R1	RESISTOR, 33k 1/4W 5%	01121	CB3335	101576	1
	R2	RESISTOR, 82k 1/4W 5%	01121	CB8235	101578	1
	R3	RESISTOR, 4.7k 1/4W 5%	01121	CB4725	101598	1
	R4	RESISTOR, 10k 1/4W 5%	01121	CB1035	101570	1
	R5	RESISTOR, 1k 1/4W 5%	01121	CB1025	101569	1
	R6	RESISTOR, 3.3k 1/4W 5%	01121	CB3325	101559	1
	R7	RESISTOR, 470Ω 1/4W 5%	01121	CB4715	101625	1
	Y1	CRYSTAL 10 MHz	52542	039483	039483	1
		SWAGE Standoff 6-32 x 1/8	88245	1530 B 1/8	100478	2

REPLACEABLE PARTS LIST

TITLE		BCD OPTION 35				
ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
		Delete Rear Panel				
		COVER PLATE 6361A	52542	057655	057655	2
		COVER PLATE 6341A & 6351A	52542	057655	057655	1
		SCREW 2-56 x 3/16 PH	96906	MS51957-2	10062503	4
		WASHER # 2 Split	96906	MS35337-77	100661	4
		Add Rear Panel				
		BCD OPTION 35 Assembly	52542	057927	057927	1
		CONNECTOR, Rect. 24 pin Female (6361A)	02660	57-40240	101177	2
		CONNECTOR, Rect. 24 pin Female (6341A & 6351A)	02660	57-40240	101177	1
		BCD CABLE & MODULE ASSEMBLY (6361A)	52542	057776	057776	2
		BCD CABLE & MODULE ASSEMBLY (6341A & 6351A)	52542	057776	057776	1
		SCREW 2-56 x 1/4 PH	96906	MS51957-3	10062504	4
		WASHER # 2 Split	96906	MS35337-77	100661	4

TITLE OPTION 35 PARALLEL BCD OUTPUT (Figure 7-22)

ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
		ASSEMBLY, BCD Module and Cable	52542	057776	057776	Ref
1		ASSEMBLY, BCD PC	52542	05770101	05770101	1
2		ASSEMBLY, Cable 25 Cond.	52542	057778	057778	1
3		ASSEMBLY, Cable 50 Cond.	52542	057777	057777	1
4		BUSHING, Snap 3/8 ID	28520	SB-562-6	117281	1
5		BUSHING, Snap 1/2 ID	28520	SB-687-8	117283	1
6		CABLE TIE	T & B	TY-24M	112488	A/R
7		BOX BCD	52542	057713	057713	1
8		COVER BCD	52542	057714	057714	1
9		SCREW PHMS 6-32 X 5/8	96906	MS51957-31	10063210	4
10		WASHER #6 Split	96906	MS35338-136	100712	4
		ASSEMBLY, BCD PC	52542	05770101	05770101	Ref
		PC BOARD	52542	057701	057701	1
		CAPACITOR, Tant 1 μF 35V	56289	150D105X9035A2	100082	1
	R1 thru R5	RESISTOR, CC 100k 1/8W 5%	01121	BB1045	101976	5
	R6 thru R8	RESISTOR, CC 10k 1/8W 5%	01121	BB1035	101697	3
	U1	IC, CMOS Hex Inverter Buffer	04713	MC14049BCP	103217	8
	U2	IC, CMOS Dual 4 Bit Latch	04713	MC14508BCP	117257	4
	U3	Same as U2				
	U4 thru U7	Same as U1				
	U8	Same as U2				
	U9	Same as U2				
	U10	Same as U1				
	U11	Same as U1				
	U12	IC, CMOS Quad 2-In AND	04713	MC14081BCP	116101	1
	U13	Same as U1				
		SPACER, Swage #6 X 1/4	71279	1247-11	100539	4
	P1	CONNECTOR, 24 Pin P/O 25 Cond Cbl	02660	57-20340	101166	1
		CABLE, 25 Cond.	70903	8459	117131	A/R
	P2	CONNECTOR, 50 Pin P/O 25 Cond Cbl	02660	57-30500	101157	1
		CABLE, 50 Cond.	70903		100112	A/R

TABLE 6.1 MANUFACTURER'S CODE-TO-NAME INDEX

00779 Amp Inc.
P.O. Box 3608, Harrisburg, PA. 17105

00853 Sangamo Electric Co., So. Carolina Div.
P.O. Box 128, Pickens, So. Carolina 29671

01121 Allen Bradley Co.
1201 S. 2nd St., Milwaukee, Wis. 53204

01295 Texas Instruments Inc.
Semiconductor & Components Div.
13500 N. Central Expressway
Dallas, Texas 75231

02114 Ferroxcube Corp.
P.O. Box 359, Mt. Marion Rd.
Saugerties, N.Y. 12477

02660 Amphenol Corp.
2801 S. 25th Ave., Broadview, IL. 60153

02735 RCA Corp., Solid State Div.
Route 202, Somerville, N.J. 08876

02768 Illinois Tool Works, Inc., Fastex Div.
195 Algonquin Rd., Des Plaines, IL. 60016

03296 Nylon Molding Corp.
40 Brown St., Springfield, N.J. 07081

03508 General Electric Company
Semiconductor Products Dept.
Electronics Park, Syracuse, N.Y. 13201

03797 Genisco Technical Corp., Eidema Div.
18435 Susana Rd., Compton, CA. 90221

03877 Transitron Electronic Corp.
168-186 Albion St., Wakefield, MA. 01880

04453 Arnolt Corp. (Code changed to 91515)
P.O. Box 540, Warsaw, IN. 46580

04713 Motorola Semiconductor, Products Div.
5005 East McDowell Rd.
Phoenix, AZ. 85008

05245 Components Corp.
2857 N. Halsted St., Chicago, IL. 60657

05464 Industrial Electronic Engineers Inc.
7720 Lemona Ave., Van Nuys, CA. 91405

05574 Viking Industries Inc.
21001 Nordhoff, Chatsworth, CA. 91311

05720 Omark Industries, Inc.
2100 S.E. Milport Rd., Portland, OR. 97222

05820 Wakefield Engineering Inc.
Audubon Rd., Wakefield, MA. 01880

06293 Cambridge Corp.
Cambridge, Mass.

06383 Panduit Corp.
17301 Ridgeland, Tinley Park, IL. 60477

06540 Amatom Electronic Hardware
Division of Mite Corp.
81 Rockdale Ave.
New Rochelle, N.Y. 10806

06560 Airco Speer Electronics
Div. of Air Reduction Co. Inc.
P.O. Box 1692, Grand Plaza
945 Grand Ave., Nogales, AZ. 85621

06776 Robinson Nugent Inc.
P.O. Box 470, New Albany, IN. 47150

07109 Oaktron Industries Inc.
704 30th St., Monroe, Wis. 53566

07126 Digitran Co.
855 S. Arroyo Parkway
Pasadena, CA. 91109

07263 Fairchild Camera & Instrument Corp.
Semiconductor Div.
313 Frontage Rd.
Mountain View, CA. 94040

07293 Bratu Engineering Co.
2048 Rascher Ave., Chicago, IL. 60625

07700 Technical Wire Products Inc.
129 Dermody St., Cranford, N.J. 07016

07933 Raytheon Co., Semiconductor Div. HQ
350 Ellis St., Mountain View, CA. 94040

08289 Blinn Delbert Co. Inc.
1678 Mission Blvd., P.O. Box 2007
Pomona, CA. 91766

08547 Wallace R. G. Co. Inc.
2301 E. Del Amo Blvd.
Compton CA. 90220

08730 Vemaline Products Co. Inc.
P.O. Box 3, 455 W. Main St.
Wyckoff, N.J. 07481

09353 C & K Components Inc.
103 Morse, Newton, Mass. 02158

11236 CTS of Berne Inc.
406 Parr Rd., Berne, IN. 46711

11237 CTS Keene Inc.
Paso Robles, CA. 93446

11879 Holloway Kenneth C. Inc.
16680 Armstrong Ave.,
Santa Ana, CA. 92705

12014 Chicago Rivet & Machine Co.
950 S. 25th Ave., Bellwood, IL. 60104

12517 Component Research Co. Inc.
1717 19th St., Santa Monica, CA. 90404

13103 Thermalloy Co.
2021 W. Valley View Lane
Dallas, TX. 75234

13715 Fairchild Camera & Instrument Corp.
Semiconductor Div., Diode Plant
4300 Redwood Hwy.
San Rafael, CA. 94903

14655 Cornell - Dubilier Electronics
Govt. Contracts Div.
150 Avenue L, Newark, N.J. 07101

14752 Electro Cube Inc.
1710 S. Del Mar Ave.
San Gabriel, CA. 91776

15513 Data Display Products
8036 Westlawn Ave.
Los Angeles, CA. 90045

15542 Mini-Circuits Laboratory
Div. of Scientific Components Corp.
2913 Quentin Rd.
Brooklyn, N.Y. 11229

15636 Elec-Trol Inc.
26477 N. Golden Valley Rd.
Saugus, CA. 91350

15818 Teledyne Semiconductor
1300 Terra Bella Ave.
Mountain View, CA. 94040

15915 Tepro of Florida Inc.
2608 Enterprise Rd.
Dunedin, FL. 33528

16179 Omni Spectra Inc.
24600 Hallwood Cr.
Farmington, MI. 48024

16258 Space Lok Inc.
2526 No. Ontario, Burbank, CA. 91504

16299 Corning Glass Works
Electronic Components Div.
3900 Electronics Div., Raleigh, NC. 27604

16428 Belden Corp.
P.O. Box 341, Richmond, IN. 47374

16733 Phelps Dodge Communications Co.
Div. of Phelps Dodge Copper Prod. Corp.
North Haven, CT. 06473

17856 Siliconix Inc.
2201 Laurelwood Rd.
Santa Clara, CA. 95054

18324 Signetics Corp.
811 E. Arques, Sunnyvale, CA. 94086

TABLE 6.1 MANUFACTURER'S CODE-TO-NAME INDEX (CONT)

18489 Reliable Capacitor Co.
7409 Bell Aire Ave.
North Hollywood, CA. 91605

18612 Vishay Resistor Products
Div. Vishay Intertechnology Inc.
68 Lincoln Hwy. Malvern, PA. 19355

19647 Caddock Electronics Inc.
3127 Chicago Ave.
Riverside, CA. 92507

19701 Mepco/Electra Inc., Electra Div.
P.O. Box 760
Mineral Wells, TX. 76067

20908 Electronic Concepts, Div. A-T-O Inc.
P.O. Box 813, Rt. 29
No. Charlottesville, VA. 22904

21192 Excelsior Hardware Co.
39 Woodland Ave., Stamford, CN. 06904

21604 Buckeye Stamping Co.
Columbus, OH. 43207

22591 Fire Control Engineering Co.
P.O. Box 2371, Fort Worth, TX. 76101

23172 Alpha Wire Corp. (New Code 92194)
Elizabeth, N.J.

23880 Stanford Applied Engineering Inc.
340 Martin Ave., Santa Clara, CA. 95050

23936 Pamotor, Div. of William J. Purdy Co.
770 Airport Blvd., Burlingame, CA. 94010

24335 Cooper Laboratories Inc.
Mystic, CT.

24655 General Radio
300 Baker Ave., Concord, MA. 01742

25088 Siemens Corp.
186 Wood Ave., S. Iselin, N.J. 08830

25120 Piezo Technology Inc.
P.O. Box 7877, 2400 Diversefield Way
Orlando, FL. 32804

25403 Amperex Electronic Corp.
Semiconductor & Microcircuits Div.
Providence Pike, Slatersville, R.I. 02876

26695 Compac Corp., Kleen-Stik Products Div.
420 Frelinghuysen Ave.
Newark, N.J. 07114

26806 American Zettler Inc.
697 Randolph Ave., Costa Mesa, CA. 92626

27014 National Semiconductor Corp.
2950 San Ysidro Way
Santa Clara, CA. 95051

27018 Optimum Designs Inc.
152 W. 42nd St., New York, N.Y. 10017

27264 Molex Products Co.
5224 Katrine Ave.
Downers Grove, IL. 60515

27556 IMB Electronic Prod. Inc.
15401 E Carmenita Rd.
Santa Fe Springs, CA. 90670

28480 Hewlett-Packard Co.
1501 Page Mill Rd., Palo Alto, CA. 94304

28520 Heyman Mfg. Co.
147 N. Michigan Ave.,
Kenilworth, N.J. 07033

29372 Tridair Industries, Fastener Division
3000 W. Lomita Blvd., Torrance, CA. 90505

29454 Monolithic Dielectrics Inc.
P.O. Box 6456, 2220 Screenland Dr.
Burbank, CA. 91505

29587 Bunker Ramo Corp., Amphenol Ind. Div
1830 S. 54th Ave., Chicago, IL. 60650

29832 Teledyne Philbrick
Allied Drive at Route 128
Dedham, MA. 02026

30146 A P Inc.
72 Corwin Dr., Painesville, OH. 44077

31433 Union Carbide Corp, Materials Systems Div.
Hwy. 276 S.E., Greenville, S.C. 29606

31918 International Electro Exchange Inc.
8081 Wallace Rd., Eden Prairie, N.M. 55343

32159 West-Cap Arizona
2201 E. Elvira Rd., Tucson, AZ. 85706

32293 Intersil Inc.
10900 N. Tantau Ave.
Cupertino, CA. 95014

32767 Griffith Plastic Corp.
1027 California Dr., Burlingame, CA. 94010

33095 Spectrum Control Inc.
152 E. Main St., Fairview, PA. 16415

34553 Amperex Electronic Corp. Component Div.
35 Hoffman Ave., Hauppauge, N.Y. 11787

44655 Ohmite Mfg. Co.
3601 W. Howard St., Skokie, IL. 60076

46384 Penn Engineering & Mfg. Corp.
Old Easton Hwy, Doylestown, PA. 18901

50522 Monsanto Co., Electronic Special Products
10131 Bubb Rd., Cupertino, CA. 95014

51181 Keytronics Inc.
707 North St., Endicott, N.Y. 13760

51495 R & D Plastics
780 32nd St., Richmond, CA. 94804

52542 Systron-Donner Corp., Instrument Div.
10 Systron Dr, Concord, CA. 94518

52648 Plessey Semiconductor
1674 McGaw Ave., Santa Ana, CA. 92705

52673 KSW Electronics Inc.
S. Bedford St., Burlingame, MA. 01803

52769 Sprague-Goodman Electronics Inc.
371 Willis Ave., Mineola, N.Y. 11501

53101 Garner Glass Co.
177 S. Indian Hill Blvd.
Claremont, CA. 91711

54453 Sullins Electronic Corp.
P.O. Box 757, 275 Pico Ave.
San Marcos, CA. 92069

56289 Sprague Electronic Co.
North Adams, MA. 01247

70485 Atlantic India Rubber Works Inc.
571 W. Polk St., Chicago, IL. 60607

70903 Belden Corp.
415 S. Kilpatrick, Chicago, IL. 60644

71279 Cambridge Thermonic Corp.
445 Concord Ave., Cambridge, MA. 01238

71286 Rexnard Inc., Specialty Fastener Div.
22 Spring Valley Rd., Paramus, N.J. 07652

71296 The Canfield Rubber Co.
Bridgeport, Conn.

71400 Bussmann Mfg., Div. of McGraw-Edison Co.
2536 W. University St.,
St. Louis, MO. 63017

71590 Globe-Union Inc., Centralab Electronics Div
5757 N. Green Bay Ave.
Milwaukee, WI. 53201

71707 Coto Coil Co. Inc.
65 Pavilion Ave., Providence, R.I. 02905

71785 TRW Electronic Components
Cinch Connector Operations
1501 Morse Ave.
Elk Grove Village, ILL. 60007

72136 Electro Motive Mfg. Co. Inc.
South Park & John Sts.
Willimantic, CO. 06226

72259 Nytronics Inc.
10 Pelham Pky., Pelham Manor, N.Y. 10803

72619 Dialight Corp.
60 Stewart Ave., Brooklyn, N.Y. 11237

72982 Erie Technological Products Inc.
644 W. 12th St., Erie, PA. 16512

73138 Beckman Instruments Inc., Helipot Div.
2500 Harbor Blvd., Fullerton, CA. 92634

73508 Brawley Felt Co.
136 West St., Northampton, MA. 01060

73803 Texas Instruments Inc.
Metallurgical Materials Div.
Attleboro, MA. 02703

73899 J F D Electronics Corp.
15th at 62nd St., Brooklyn, N.Y. 11219

73957 Groov-Pin Corp.
1125 Hendricks Causeway
Ridgefield, N.J. 07657

74370 Birtcher Corp., Manning Instrument Div.
4371 Valley Blvd.
Monterey Park, CA. 90032

74542 Hoyt Electrical Instrument Inc.
45 Washington St., Penacook, N.H. 03301

74970 E.F. Johnson Co.
299 10th Ave., S.W., Waseca, MN. 56093

75042 TRW Electronic Components
Fixed Resistors Philadelphia Div.
401 N. Broad St., Philadelphia, PA. 19108

75915 Littlefuse Inc.
800 E. Northwest Hwy.
Des Plaines, IL. 60016

76381 Minnesota Mining and Mfg. Co.
3 M Center, St. Paul, Minn. 55101

76854 Oak Industries Inc., Switch Div.
S. Main St., Crystal Lake, IL. 60014

77969 Rubbercraft Corp. of Calif. Ltd.
1800 W. 220th St., Torrance, CA. 90507

78189 Illinois Tool Works Inc., Shakeproof Div.
St. Charles Rd., Elgin IL. 60120

78553 Tinnerman Products Inc.
8700 Brookpark Rd., Cleveland, OH. 44129

79727 C-W Industries
P.O. Box 96, 550 Davisville Rd.
Warminister, PA. 18974

79963 Zierick Mfg. Co.
Radio Circle, Mt. Kisco, N.Y. 10549

80294 Bourns Inc., Instrument Div.
6135 Magnolia Ave.
Riverside, CA. 92506

81073 Grayhill Inc.
561 Hillgrove Ave., La Grange, IL. 60525

81312 Litton Industries Inc., Winchester Elec. Div.
Main St & Hillside Ave.
Oakville, CT. 06779

81349 MIL STD

81483 International Rectifier Corp.
9220 Sunset Blvd., Los Angeles, CA. 90069

82389 Switchcraft Inc.
5555 N. Elston Ave., Chicago, IL. 60630

83014 Hartwell Corp.
9035 Venice Blvd., Los Angeles, CA.90034

83330 Smith, Herman H. Inc.
812 Snediker Ave., Brooklyn, N.Y. 11207

83781 National Electronics Inc. Varian Division
P.O. Box 269, Geneva, IL. 60134

86445 Penn Fibre & Specialty Co.
2032 E. Westmoreland St.
Philadelphia, PA. 19134

86928 Seastrom Mfg. Co. Inc.
701 Sonora Ave., Glendale, CA. 91201

88245 Litton Systems Inc.
13536 Saticoy St., Van Nuys, CA. 91409

89110 Amp Inc.
P.O. Box 3608, Harrisburg, PA. 17105

89826 Radiation Internation Inc.
Portland Heavy Industries Div.
P.O. Box 20296, 19000 N.E. Sandy Blvd.
Portland, OR. 97220

90201 Mallory Capacitor Co.
P.O. Box 372, 3029 E. Washington St.
Indianapolis, IN. 46206

91418 Radio Materials Co.
4242 W. Bryn Mawr, Chicago, IL. 60646

91506 Augat Inc.
33 Perry Ave., Attleboro, MA. 02703

91515 Arnolt Corp.
P.O. Box 540, Warsaw, IN. 46580

91537 Magazines For Industry Inc.
777 3rd Ave., New York, N.Y. 10017

91637 Dale Electronics Inc.
P.O. Box 609, Columbus, N.E. 68601

91673 Epiphone Inc.
New York, N.Y.

91737 ITT Cannon/German
922 So. Lyon St., Santa Ana, CA. 92705

91836 Kings Electronics Co. Inc.
40 Marbledale Rd., Tuckahoe, N.Y. 10707

92194 Alpha Wire Corp.
Elizabeth, N.J.

92702 IMC Magnetics Corp., Eastern Div.
570 Main St.,
Westbury Long Island, N.Y. 11591

93907 Camcar Screw & Manufacturing Co.
600 18th Ave., Rockford, IL. 61101

94222 Southco Inc.
Lester, PA. 19113

95263 Leecraft Mfg. Co. Inc.
21-16 44th Rd.
Long Island City, N.Y. 11101

95348 Gordos Corp.
250 Glenwood Ave.
Bloomfield, N.J. 07003

95987 Weckesser Co. Inc.
4444 W. Irving Park Rd.
Chicago, IL. 60641

96067 Microwave Associates West
999 E. Arques Ave., Sunnyvale, CA. 94086

96906 MIL STD

96987 Benesh Tool and Mfg. Co.
1910 N. Telegraph, P.O. Box 906
Monroe, MI. 48161

98291 Sealectro Corp.
225 Hoyt, Mamaronick, N.Y. 10544

98921 O and M Mfg. Co.
8203 Market St. Rd., Houston, TX. 77029

98978 International Electronic Research Corp.
135 W. Magnolia Ave., Burbank, CA. 91502

99515 Marshall Industries Capacitor Div.
Monrovia, CA.

99392 S T M Corp.
2904 Chapman St., Oakland, CA. 94601

99800 American Precision Industries Inc.
Delevan Div.
270 Quaker Rd., E. Aurora, N.Y. 14052

CHAPTER 7

DRAWINGS

7.1 INTRODUCTION

This chapter contains the final assembly and schematic drawings for the Model 63X1A Series Frequency Counters. The schematic diagrams relate to the detailed circuit descriptions located in Chapter 4 of this manual. The parts list contained in Chapter 6 relate to the reference designation callouts on the diagrams. Table 7-1 provides a list by figure number of the drawings, with title, drawing number and manual page number.

TABLE 7-1 LIST OF DRAWINGS

Figure No.	Drawing Title	Drawing No.	Page No.
7-1	Model 63X1A Test Assembly	057833	7-3
7-2	Model 63X1A Front Panel Assembly	057832	7-4
7-4	Model 63X1A Rear Panel Assembly	057736	7-4
7-4	Model 63X1A Universal Assembly	057831	7-5
7-5	Model 63X1A Mother Board P.C. Assembly	05747401	7-6
7-6	Model 6341A Block Diagram Schematic	7-057840	7-7
7-7	Model 6351A Block Diagram Schematic	7-057837	7-8
7-8	Model 6361A Block Diagram Schematic	7-057834	7-9
7-9	Model 6341A, A1, Display P.C. Assembly	05747503	7-10
7-10	Model 6351A, A1, Display P.C. Assembly	05747502	7-11
7-11	Model 6361A, A1, Display P.C. Assembly	05747501	7-12
7-12	Model 63X1A, A1, Display P.C. Assembly Schematic	7-05747501	7-13
7-13	A2, 100 MHz Amplifier Right Assembly	057720	7-14
7-14	A4, 100 MHz Amplifier Left Assembly	057721	7-15
7-15	A2 & A4 100 MHz Amplifier P.C. Assembly	05747701	7-16
7-16	A2 & A4 100 MHz Amplifier P.C. Assembly Schematic	7-05747701	7-17
7-17	Decade P.C. Assembly	05745701	7-18
7-18	A3 & A5 Decade P.C. Assembly Schematic	7-05745701	7-19
7-19	10 MHz Oscillator P.C. Assembly	05708801	7-20
7-20	10 MHz Oscillator P.C. Assembly Schematic	7-05708801	7-21
7-21	Model 6341A & 6351A Option 35 BCD Cable And Module Assembly Schematic	7-0577010	7-22
7-22	Option 35 BCD Cable & Module Assembly	057776	7-23
7-23	Option 35 Cable Assembly 25 Conductor	057778	7-23
7-24	Option 35 Cable Assembly 50 Conductor	057777	7-23
7-25	Option 35 BCD P.C. Assembly	05770101	7-23

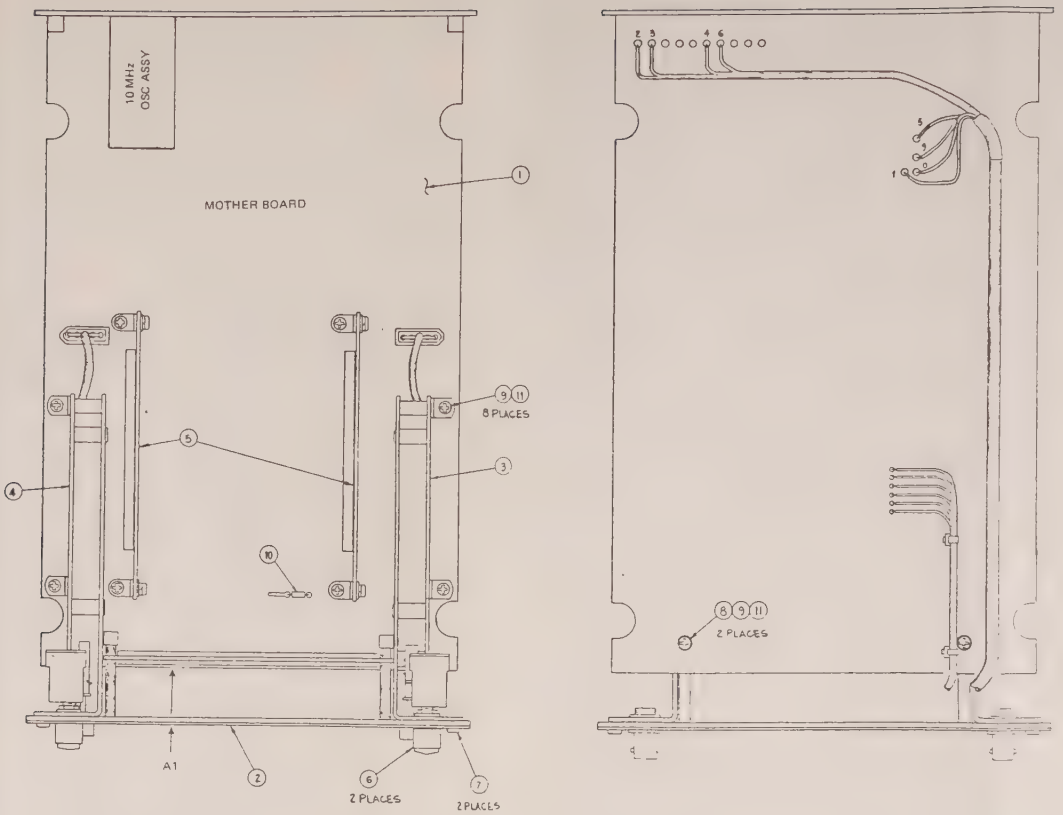


FIGURE 7-1
MODEL 6361A TEST ASSEMBLY
#057833 REV A

NOTE
Used on 6361A only

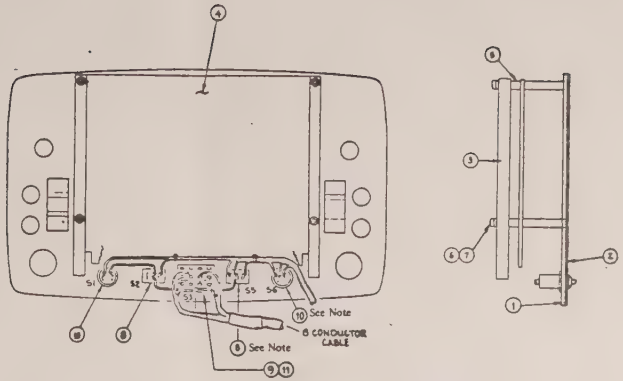


FIGURE 7-2
MODEL 63X1A FRONT PANEL
#057832

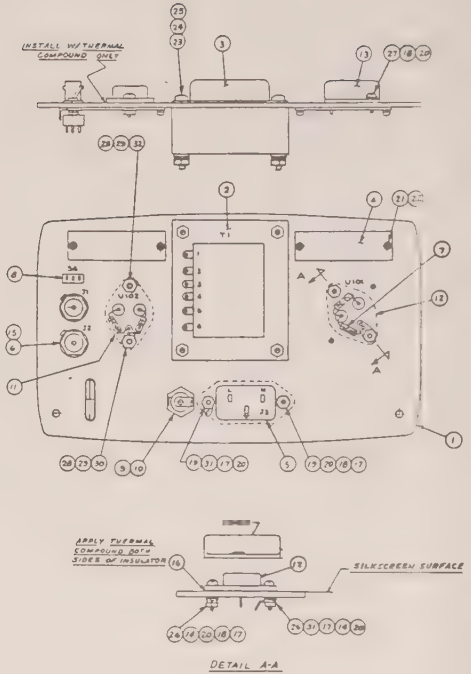


FIGURE 7-3
MODEL 63X1A
REAR PANEL ASSEMBLY
#057736 REV B

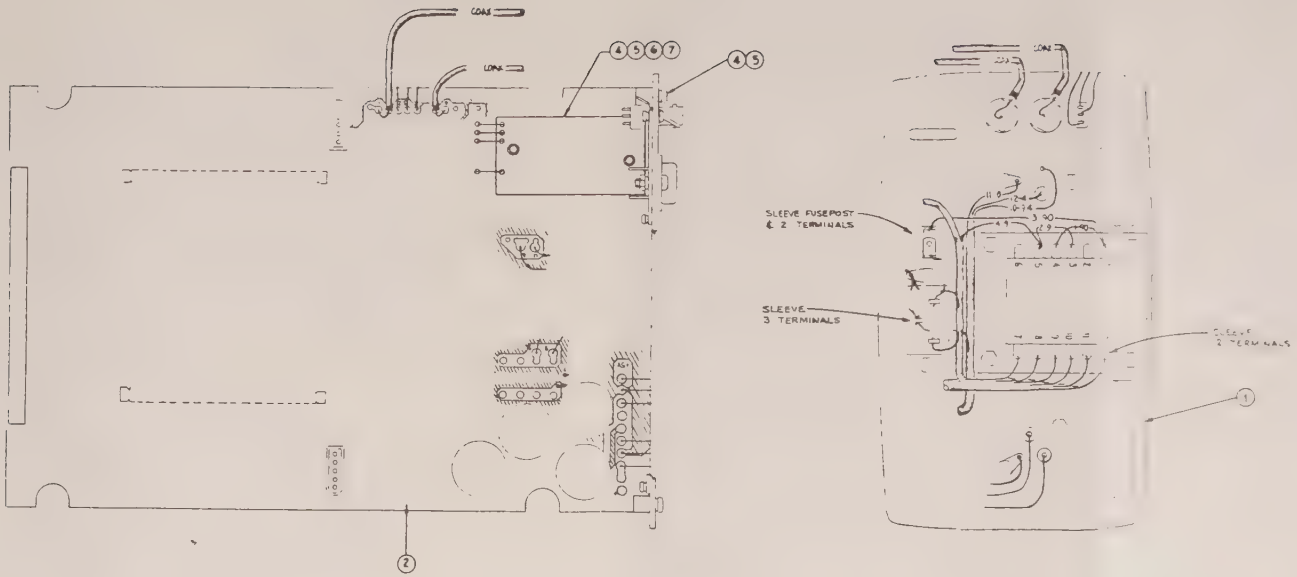


FIGURE 7-4
MODEL 63X1A UNIVERSAL ASSEMBLY
#057831 REV A_2

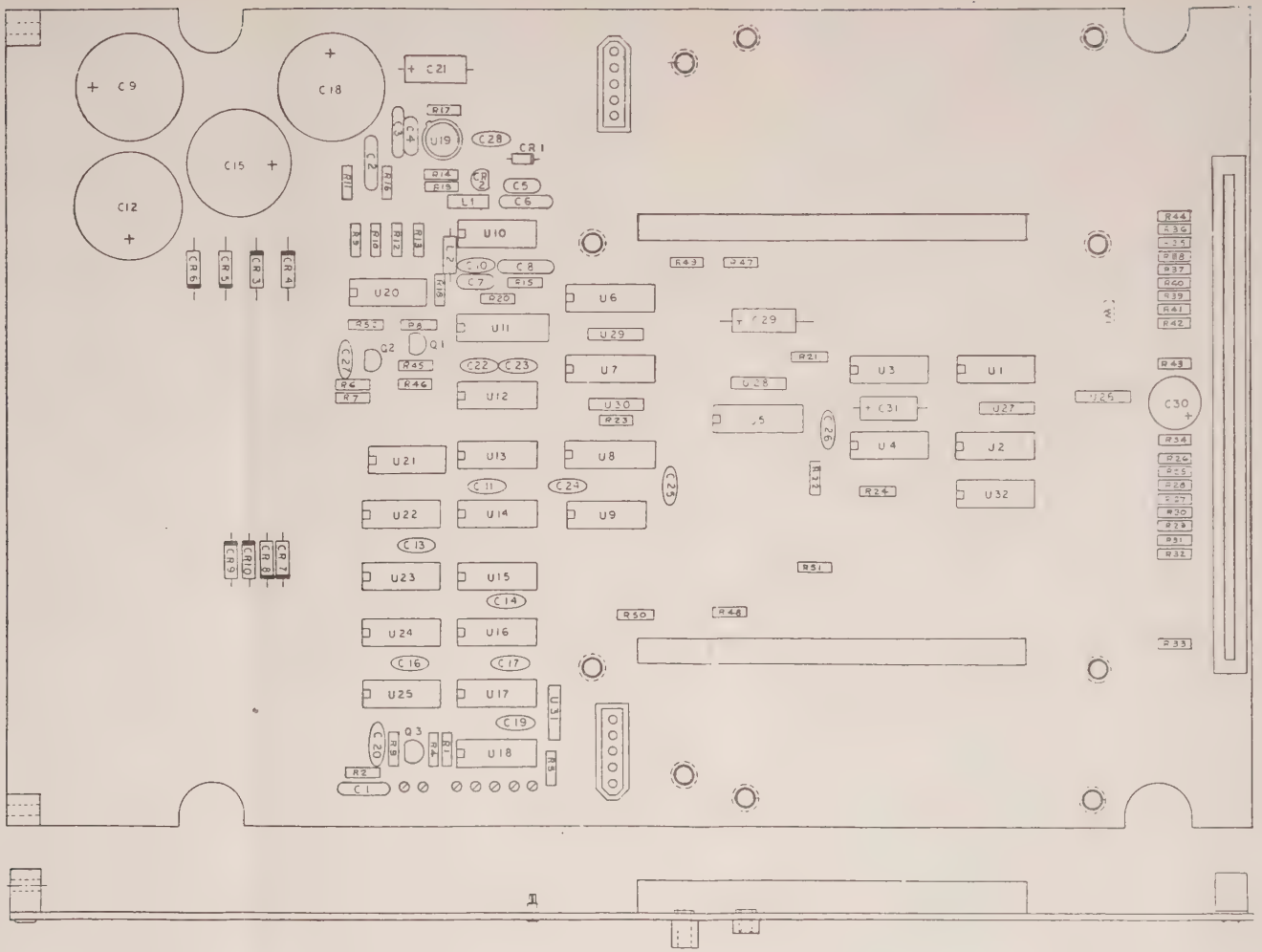


FIGURE 7-5
MODEL 63X1A MOTHER BOARD
P.C. ASSEMBLY
=05747401 REV A1

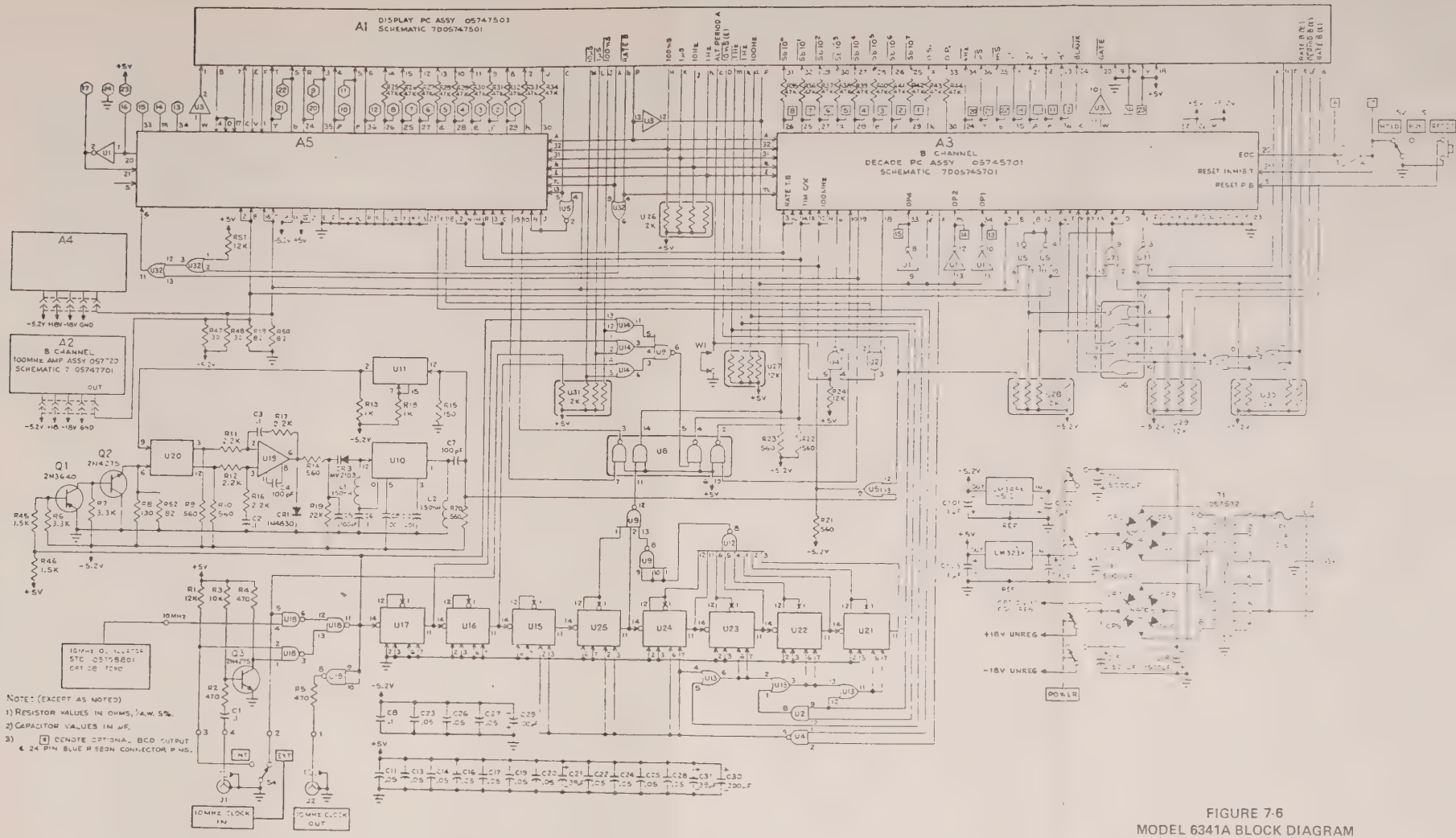


FIGURE 7-6
MODEL 6341A BLOCK DIAGRAM
SCHEMATIC #7-057840 REV B

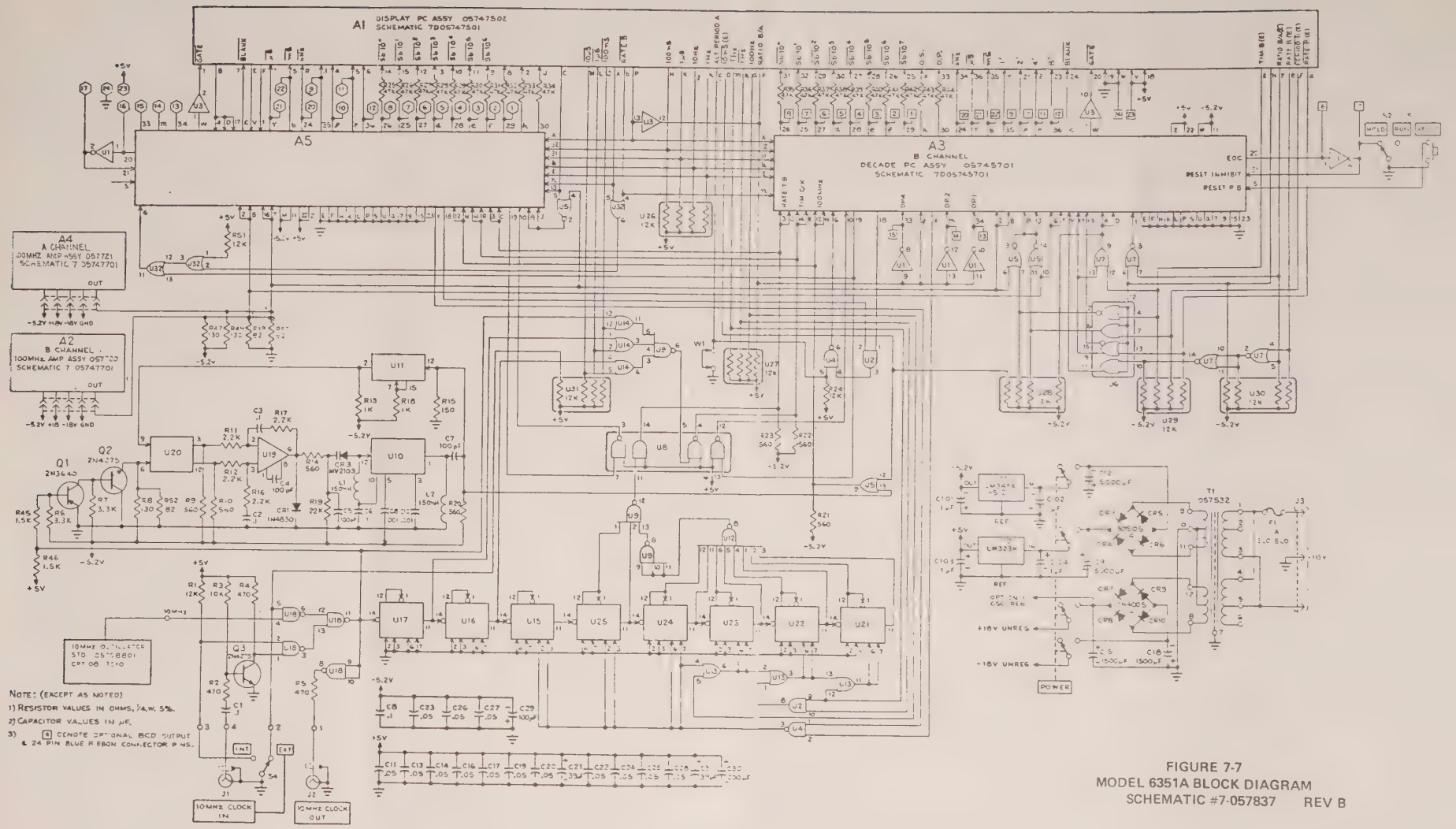


FIGURE 7-7
MODEL 6351A BLOCK DIAGRAM
SCHEMATIC #7-057837 REV B

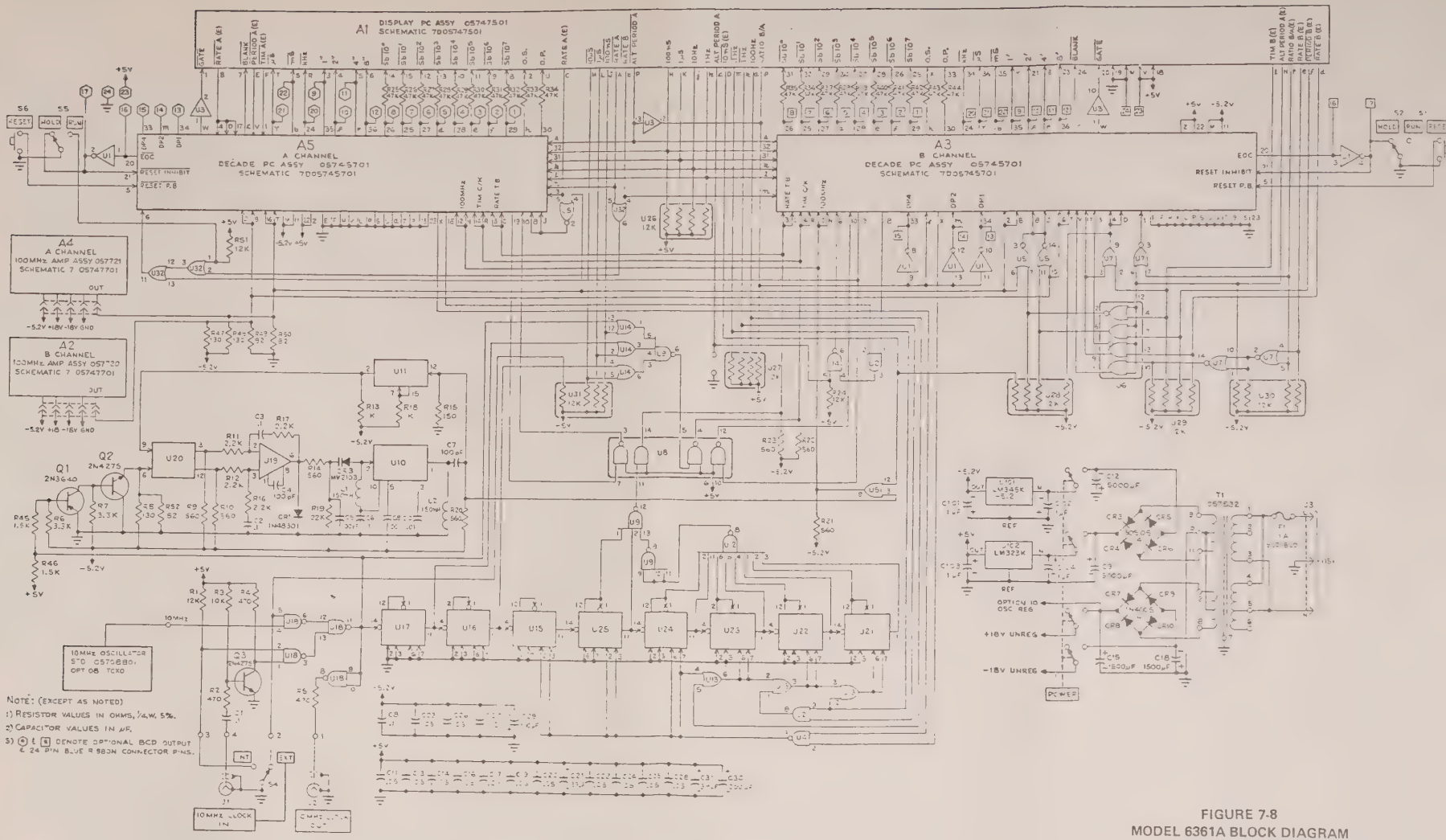


FIGURE 7-8
MODEL 6361A BLOCK DIAGRAM
SCHEMATIC #7-057834 REV B

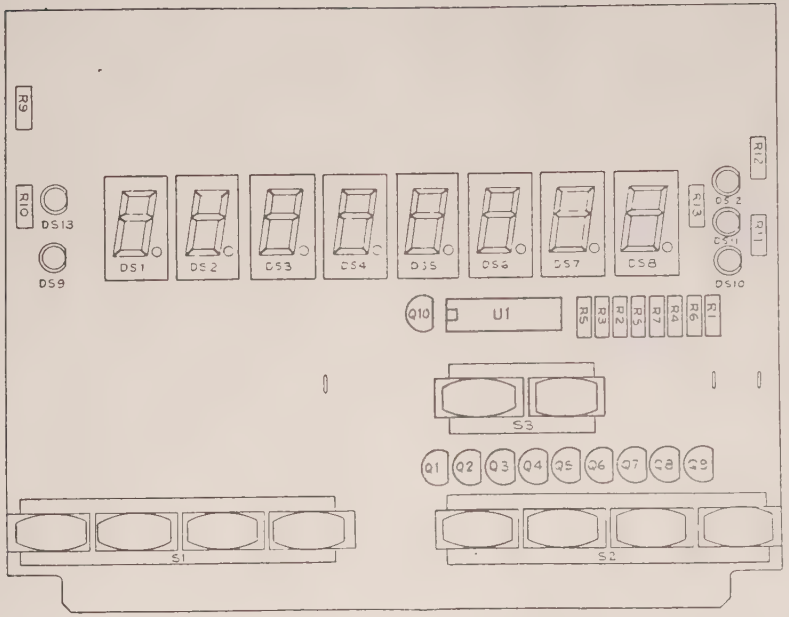


FIGURE 7-9
MODEL 6341A
A1, DISPLAY P.C. ASSEMBLY
=05747503 REV B

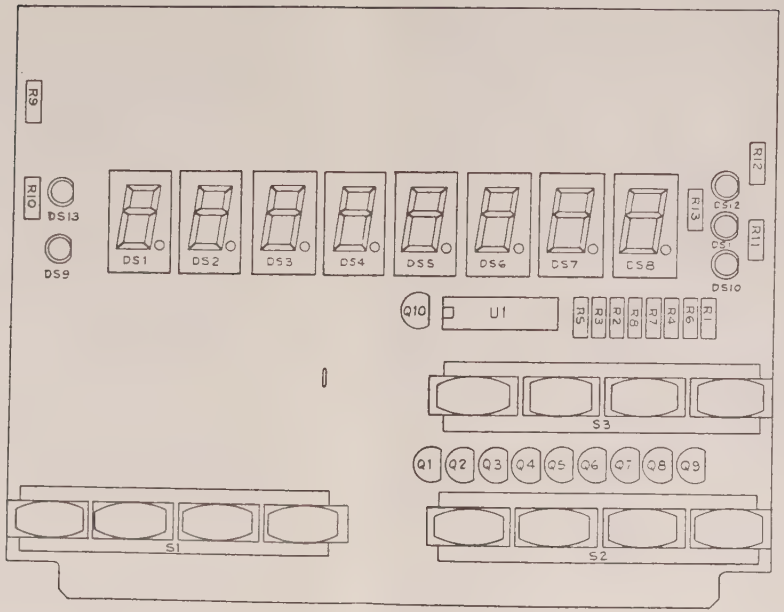


FIGURE 7-10
MODEL 6351A
A1, DISPLAY P.C. ASSEMBLY
#05747502 REV B

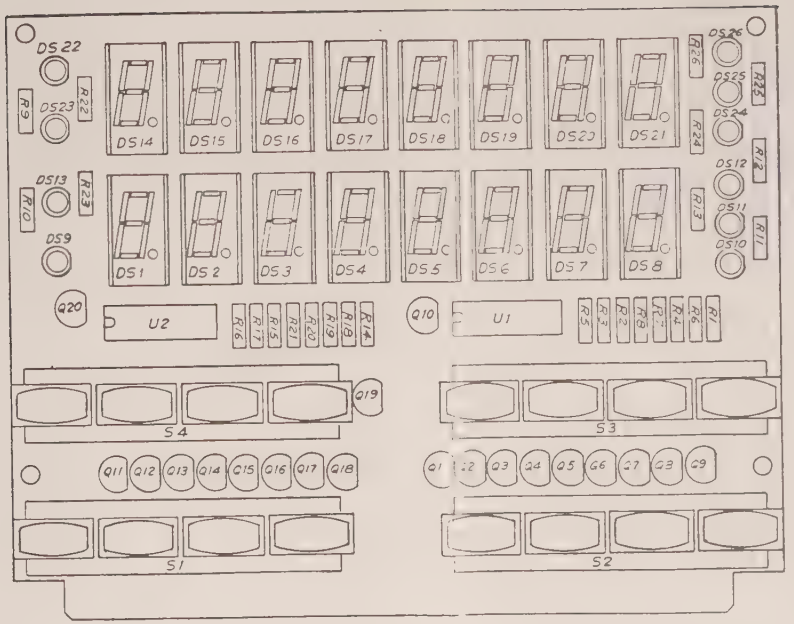
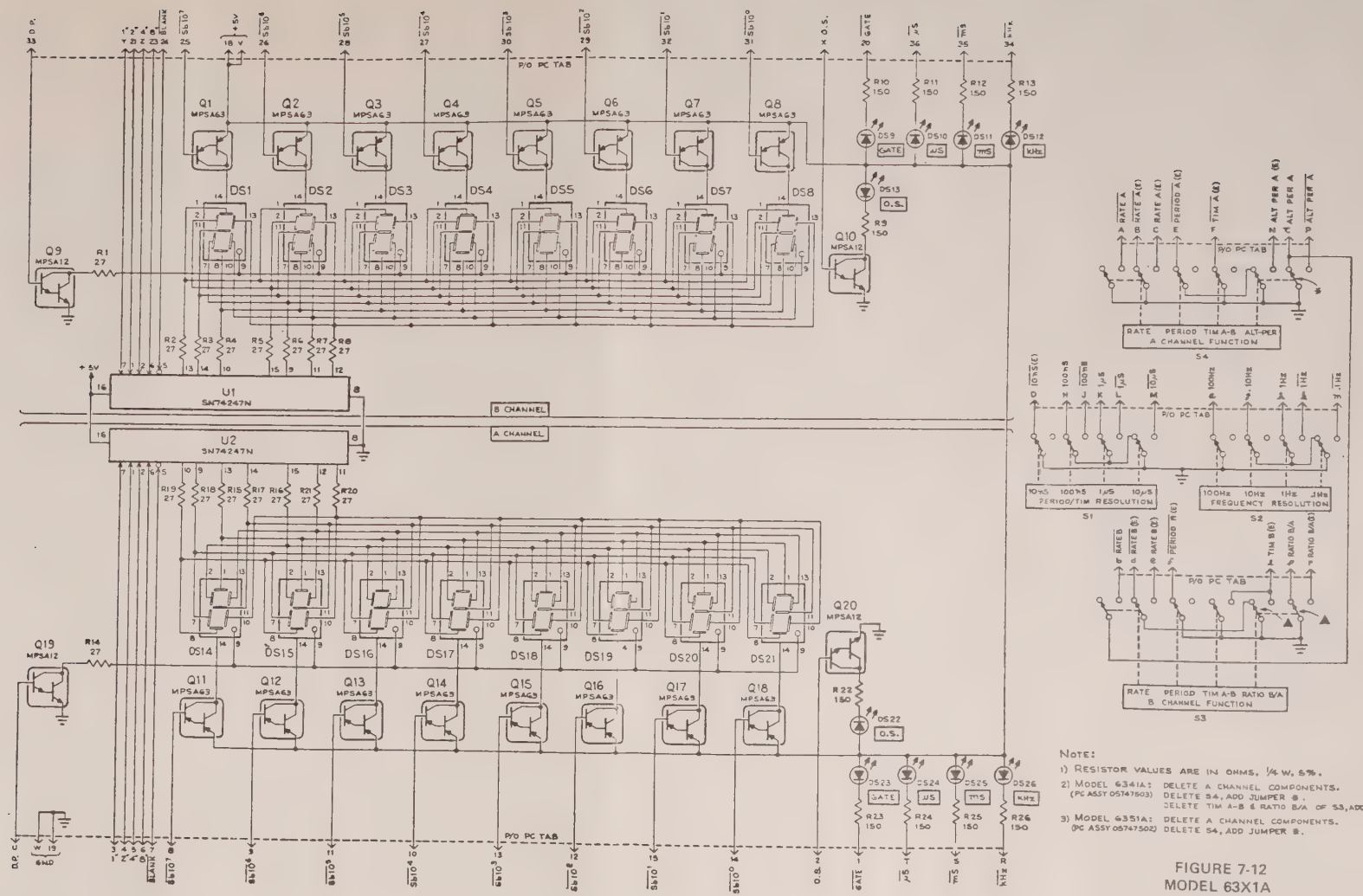


FIGURE 7-11
MODEL 6361A
A1, DISPLAY P.C. ASSEMBLY
#05747501 REV B



Note:

1) Resistor values are in ohms, ¼ w, 5%.

2) Model 6341A: (PC Assy 05747503) Delete A channel components. Delete S4, add jumper B. Delete TIM A-B & RATIO B/A of S3, add 2 jumpers ▲.

3) Model 6351A: (PC Assy 05747502) Delete A channel components. Delete S4, add jumper B.

FIGURE 7-12
MODEL 63X1A
A1, DISPLAY P.C. ASSEMBLY
SCHEMATIC #7-05747501 REV C

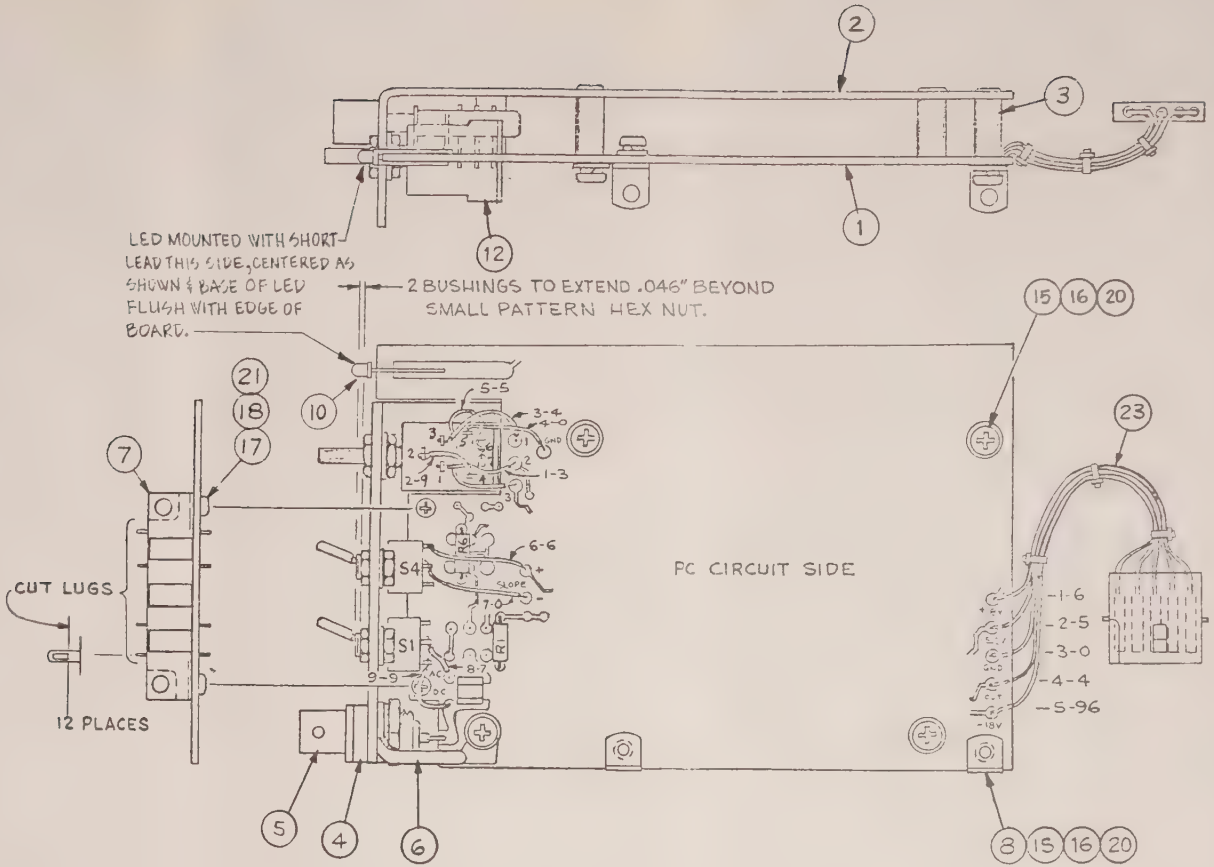


FIGURE 7-13
A2, 100 MHz AMPLIFIER RIGHT ASSEMBLY
#057720 REV C

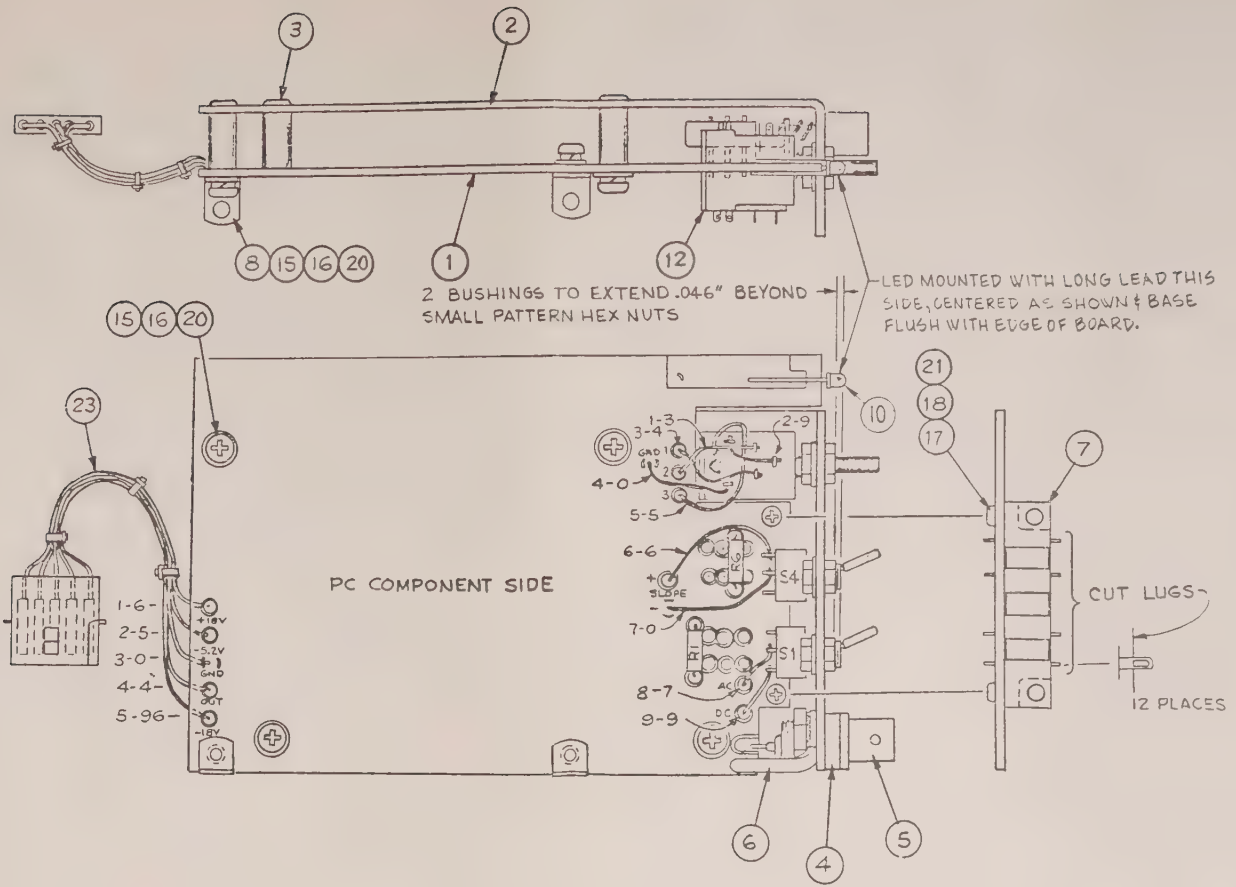


FIGURE 7-14
A4, 100 MHz AMPLIFIER LEFT ASSEMBLY
#057721 REV C

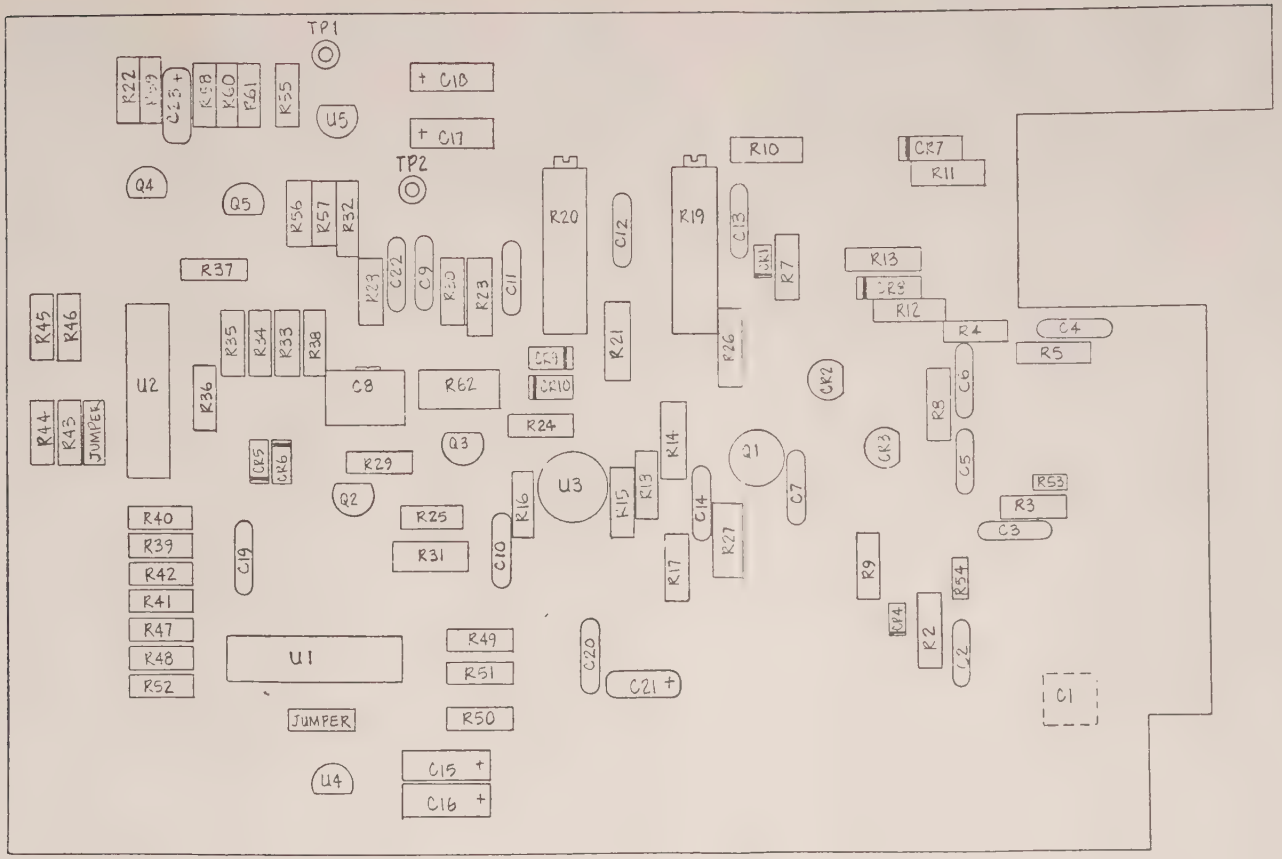


FIGURE 7-15
A2 & A4 100 MHz AMPLIFIER P.C. ASSEMBLY
#05747701 REV C

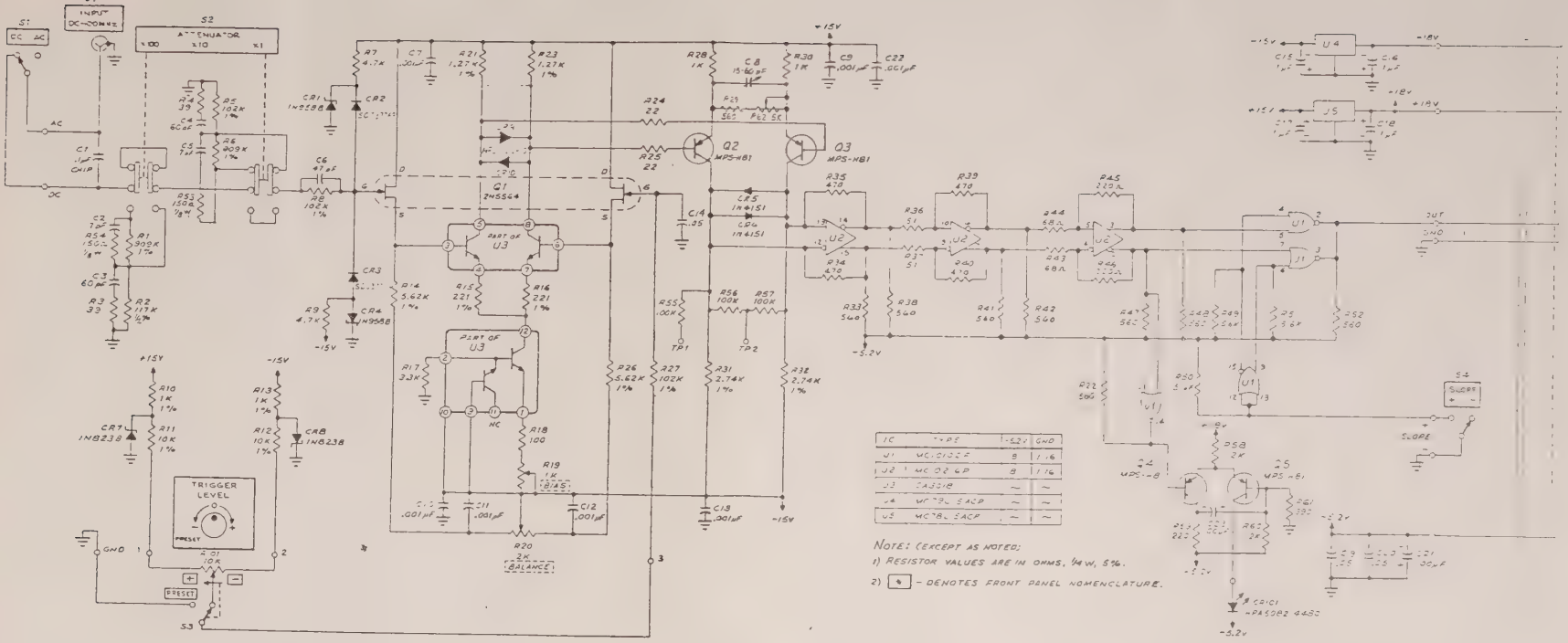


FIGURE 7-16
A2 & A4 100 MHz AMPLIFIER ASSEMBLY
SCHEMATIC #7-05747701 REV C

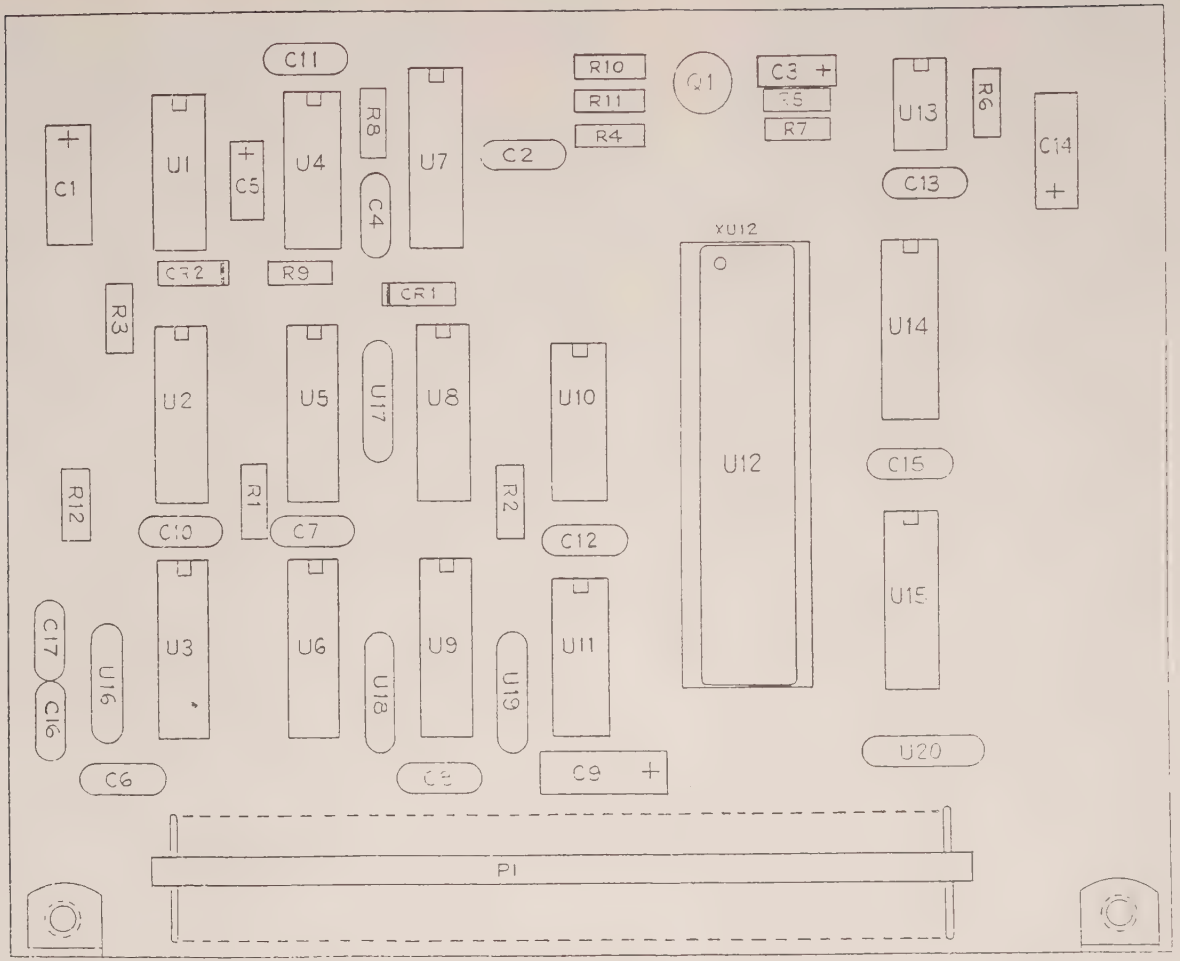


FIGURE 7-17
DECADE PC ASSEMBLY
=05745701 REV B

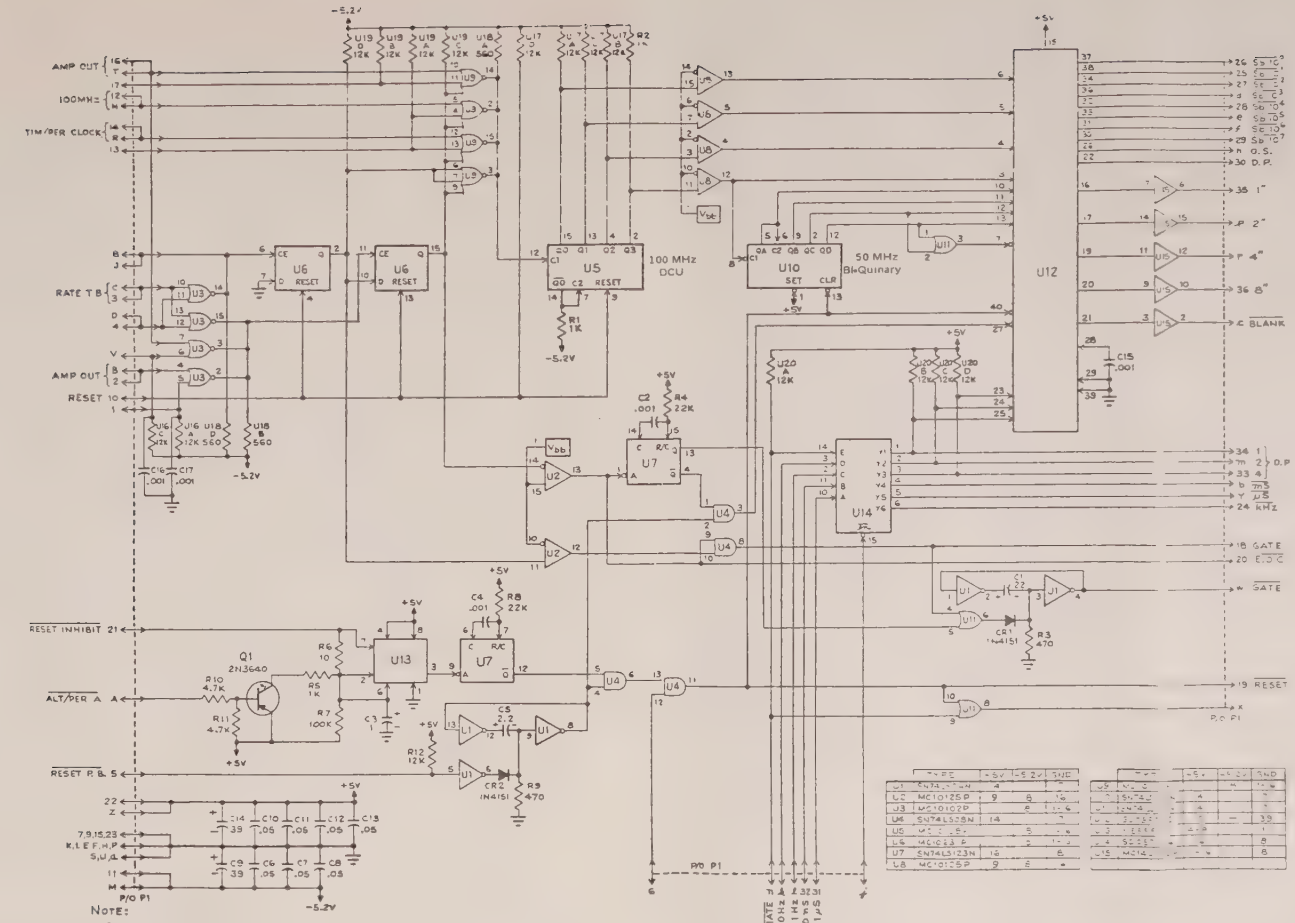


FIGURE 7-18
A3 & A5 DECADE PC ASSEMBLY
SCHEMATIC #7-05745701 REV B

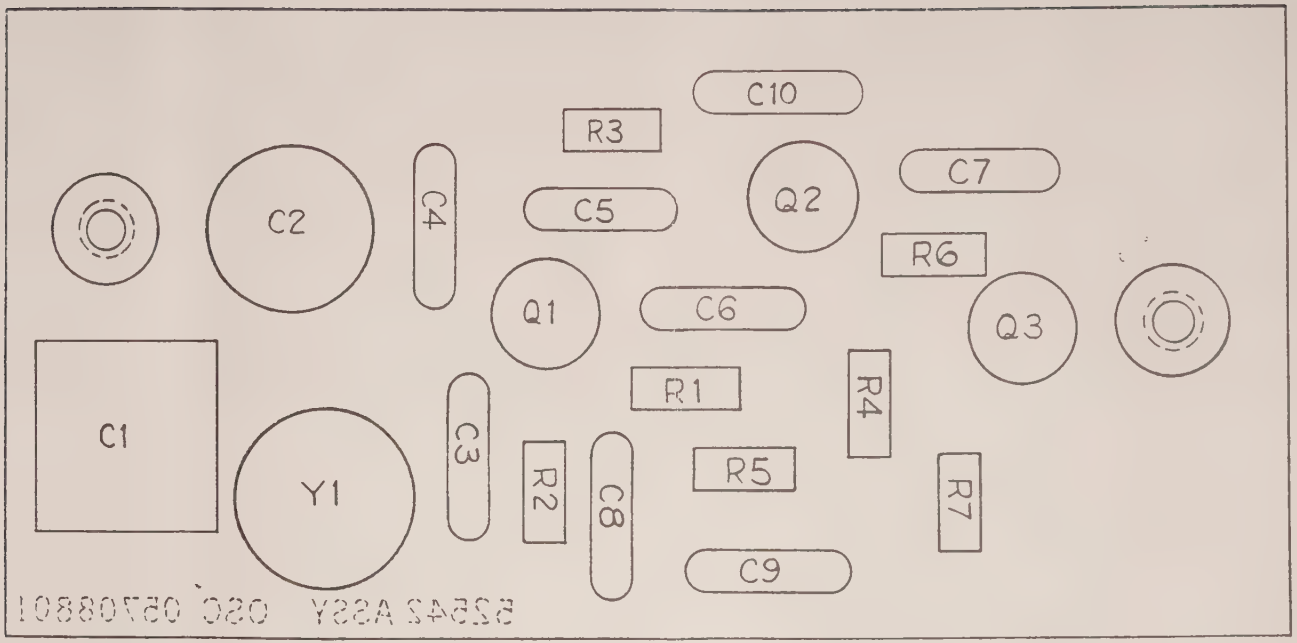
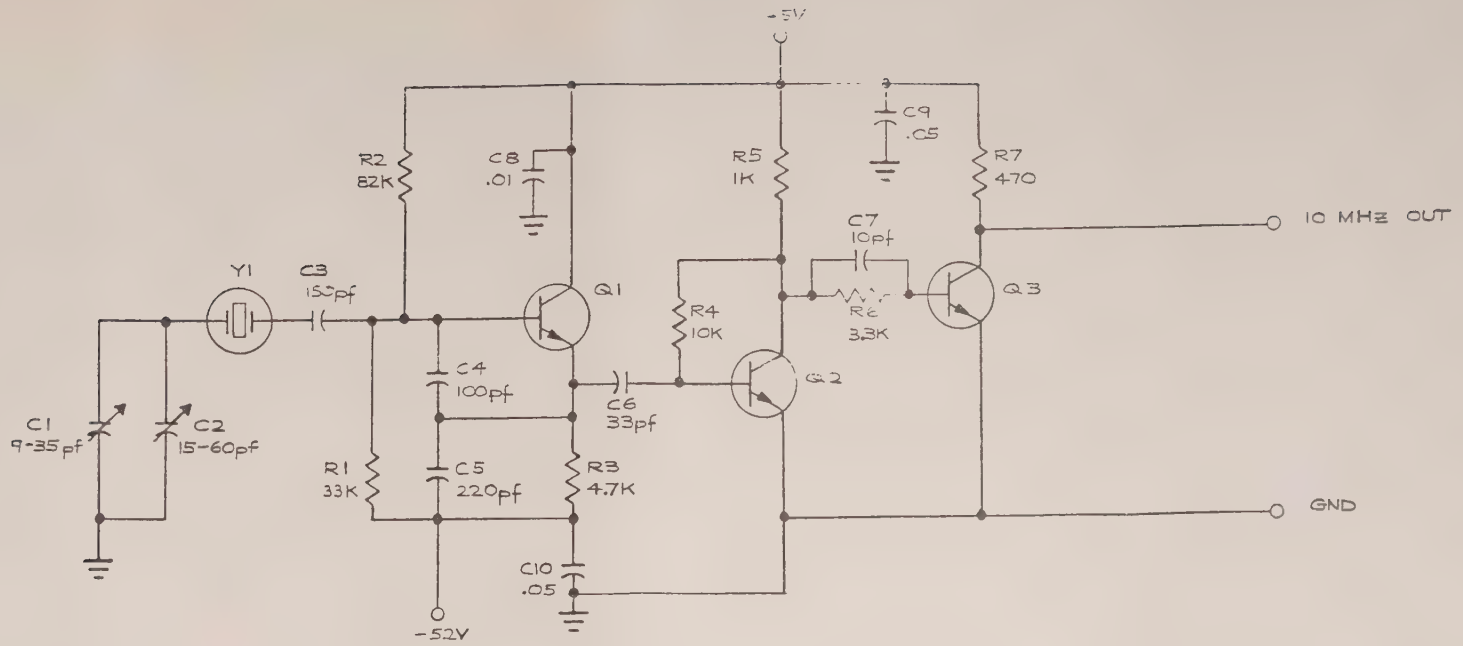
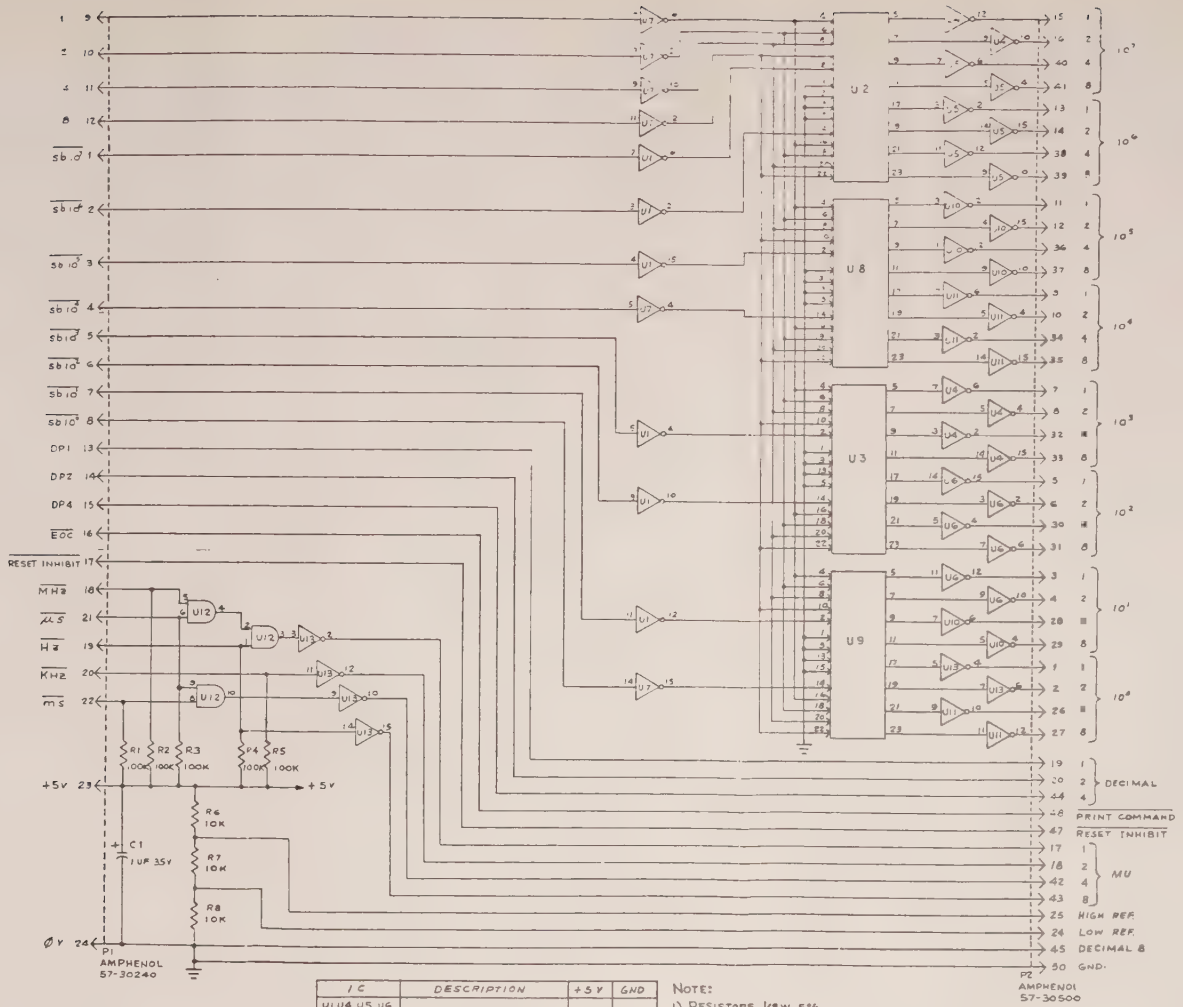


FIGURE 7-19
10 MHz OSCILLATOR PC ASSEMBLY
=05708801 REV A



3. ALL TRANSISTOR TYPES ARE 2N4275
2. ALL RESISTOR VALUES ARE IN Ω
1. ALL CAPACITORS ARE IN μf
NOTES: UNLESS OTHERWISE SPECIFIED

FIGURE 7-20
10 MHz OSCILLATOR PC ASSEMBLY
SCHEMATIC 7-05708801 REV A



IC	DESCRIPTION	+5V	GND
U1, U4, U5, U6, U7, U10, U11, U13	MC 14049B CP	1	8
U12	MC 14081B CP	14	7
U2, U3, U8, U9	MC 14508B CP	24	12

NOTE:
1) RESISTORS 1/8W, 5%.

MU TRANSLATION

BINARY 1 = MHz
BINARY 2 = KHz
BINARY 4 = mS
BINARY 5 = µS
BINARY 9 = Hz

FIGURE 7-21
MODEL 6341A & 6351A
OPTION 35
BCD CABLE & MODULE ASSEMBLY
SCHEMATIC #7-0577010 REV A

63X1A-4-77

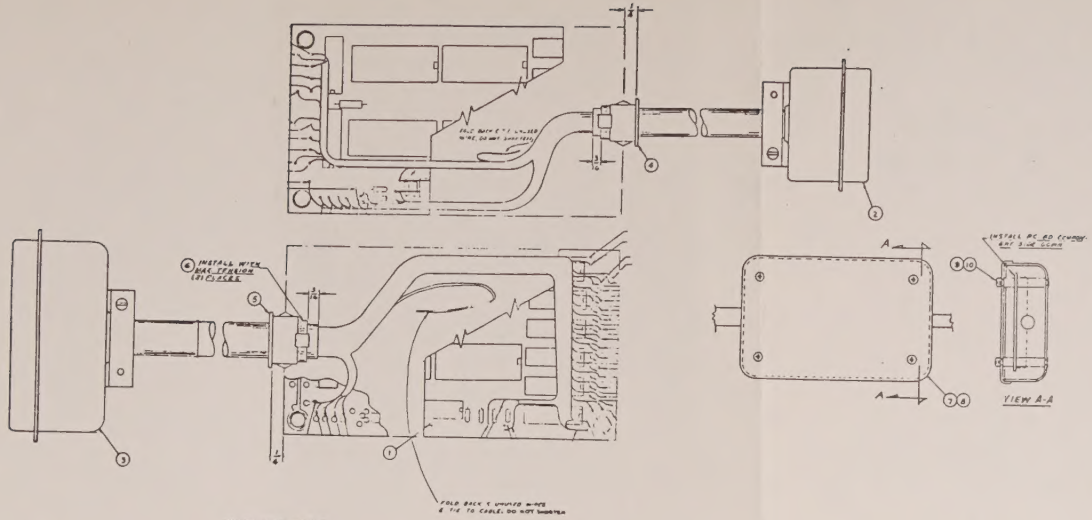


FIGURE 7-22
OPTION 35
BCD CABLE & MODULE ASSEMBLY
#057776

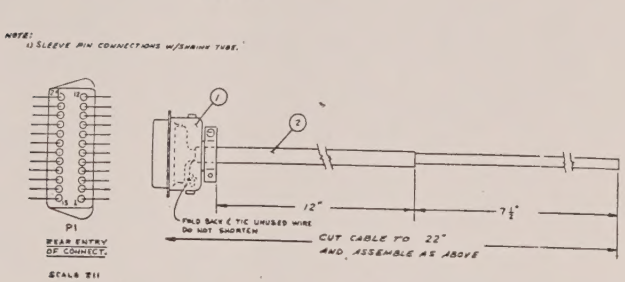


FIGURE 7-23
OPTION 35
CABLE ASSEMBLY 25 COND.
#057778

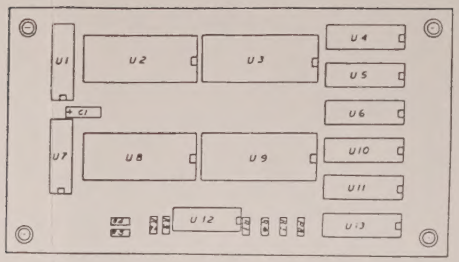


FIGURE 7-25
OPTION 35
BCD PC ASSEMBLY
=05770101

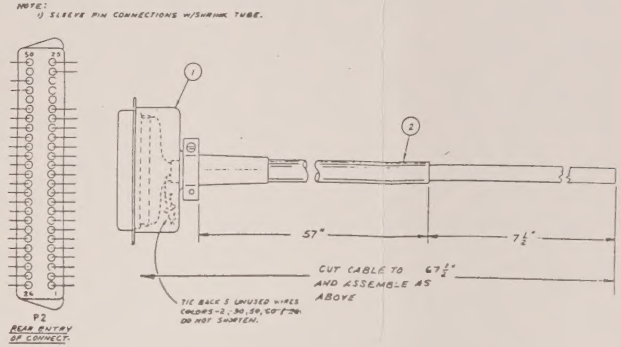


FIGURE 7-24
OPTION 35
CABLE ASSEMBLY 50 COND.
=057777

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